L'architecture
Processeurs ARM

ARM: (Advanced RISC Machines)

Produit des Architectures de cœur
De microprocesseur

- Fujitsu
- Texas instrument
- ST Microelectronics

Différents types d'architecture
De cœur de microprocesseur

- ARM7
- ARM9 10 & 11
- A, M, & R

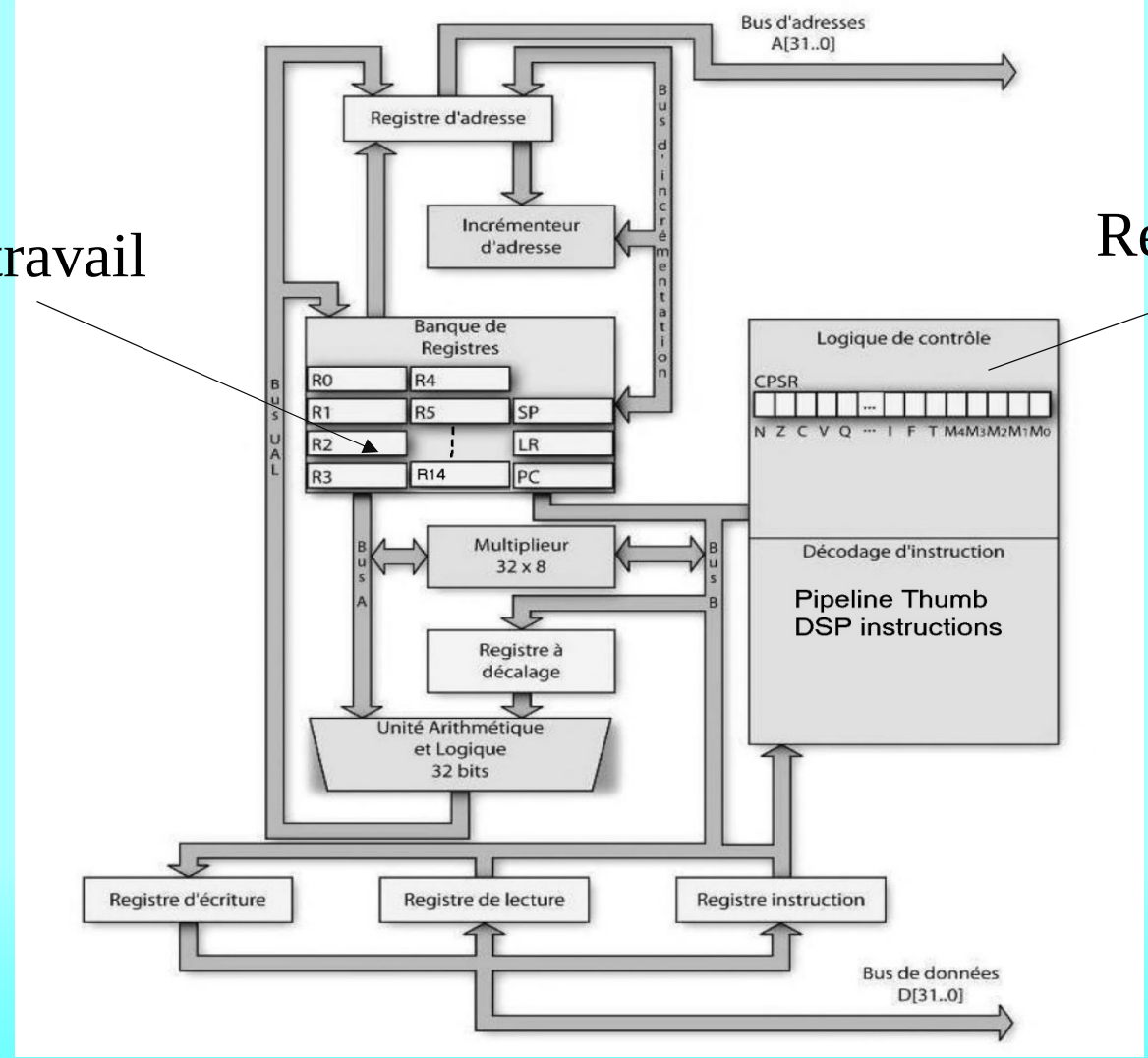
Applications → Téléphone mobile, console jeux,
Systèmes Embarqués ….

Architecture RISC
(Jeux d'instructions réduit)

Une instruction s'exécute
En un cycle machine

Registre de travail

Registre d'état

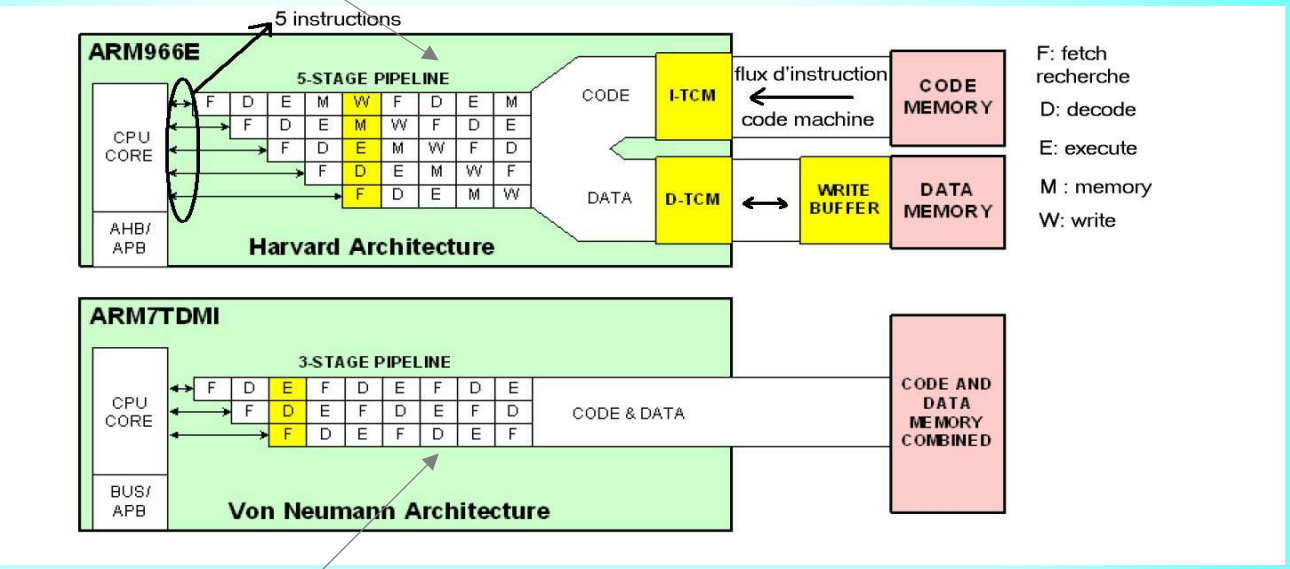


Architecture PIPELINE
Exécution de plusieurs instruction à la fois

5 étages (pipeline): 5 instructions en même temps

Cœur ARM966E

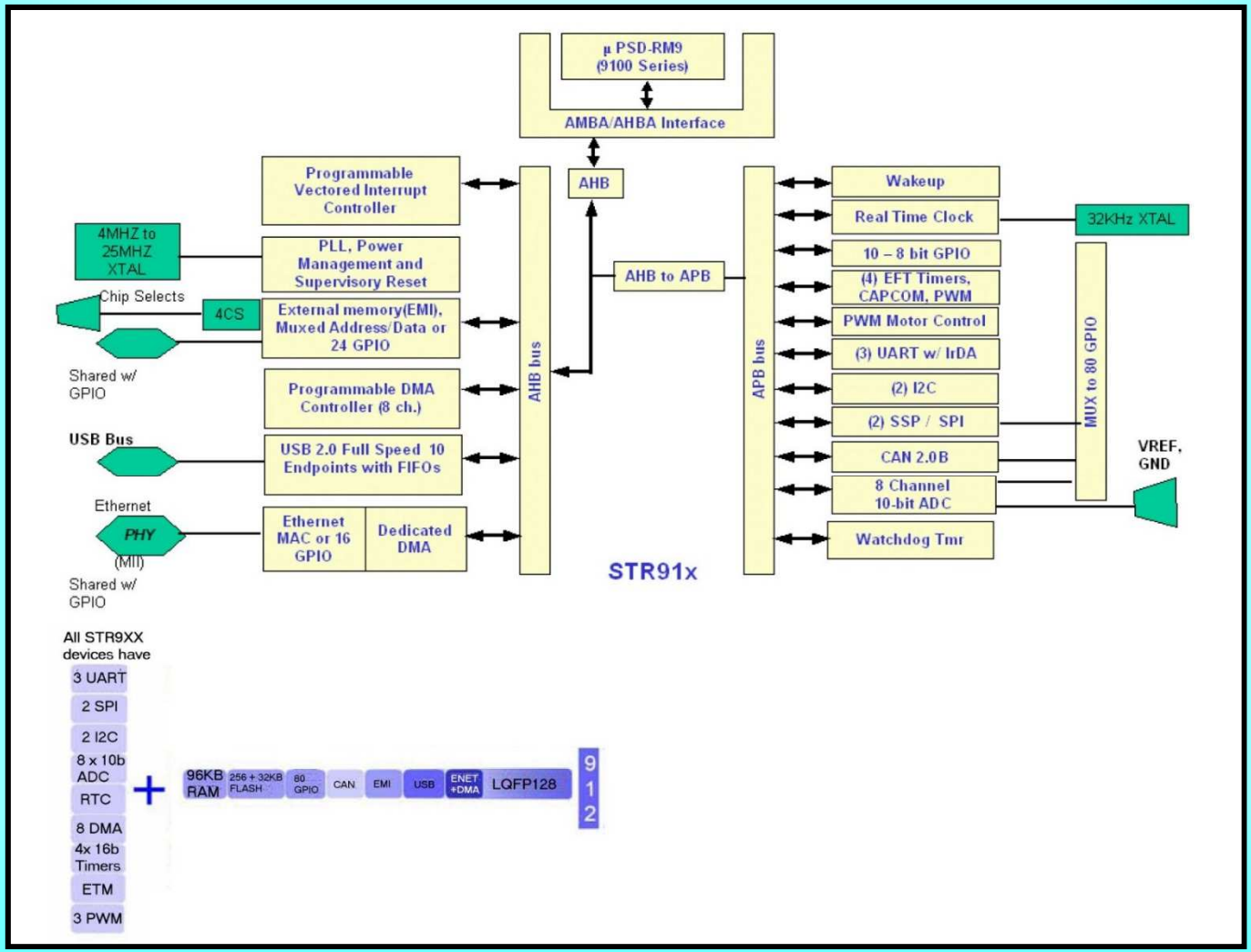
Cœur ARM 7TDMI



3 étages (pipeline) : 3 instructions en même temps

Processeur utilisé STR912
(ST Microelectronic) → Cœur ARM9

Microcontrôleur

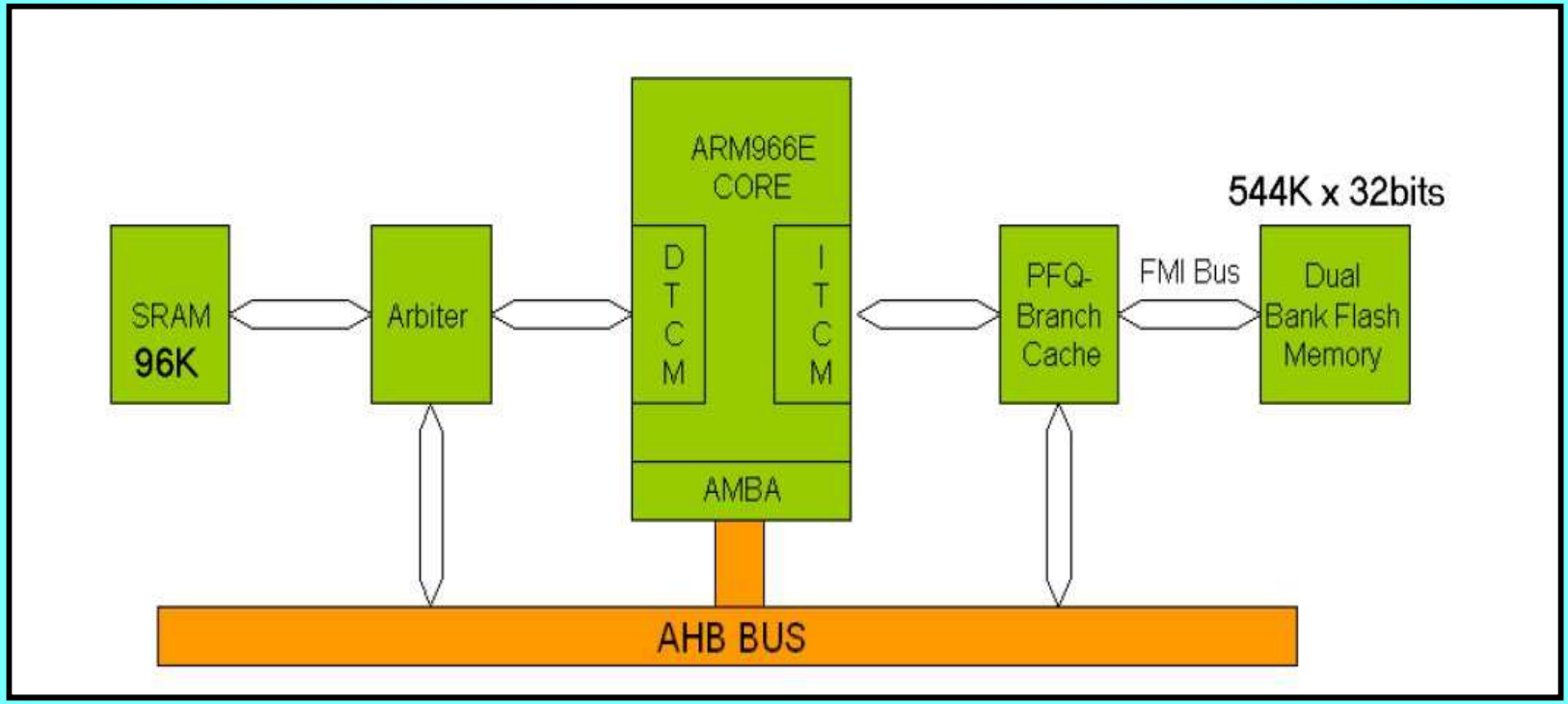


Processeur utilisé STR912
(ST Microelectronic)

Intégration mémoire programme FLASH

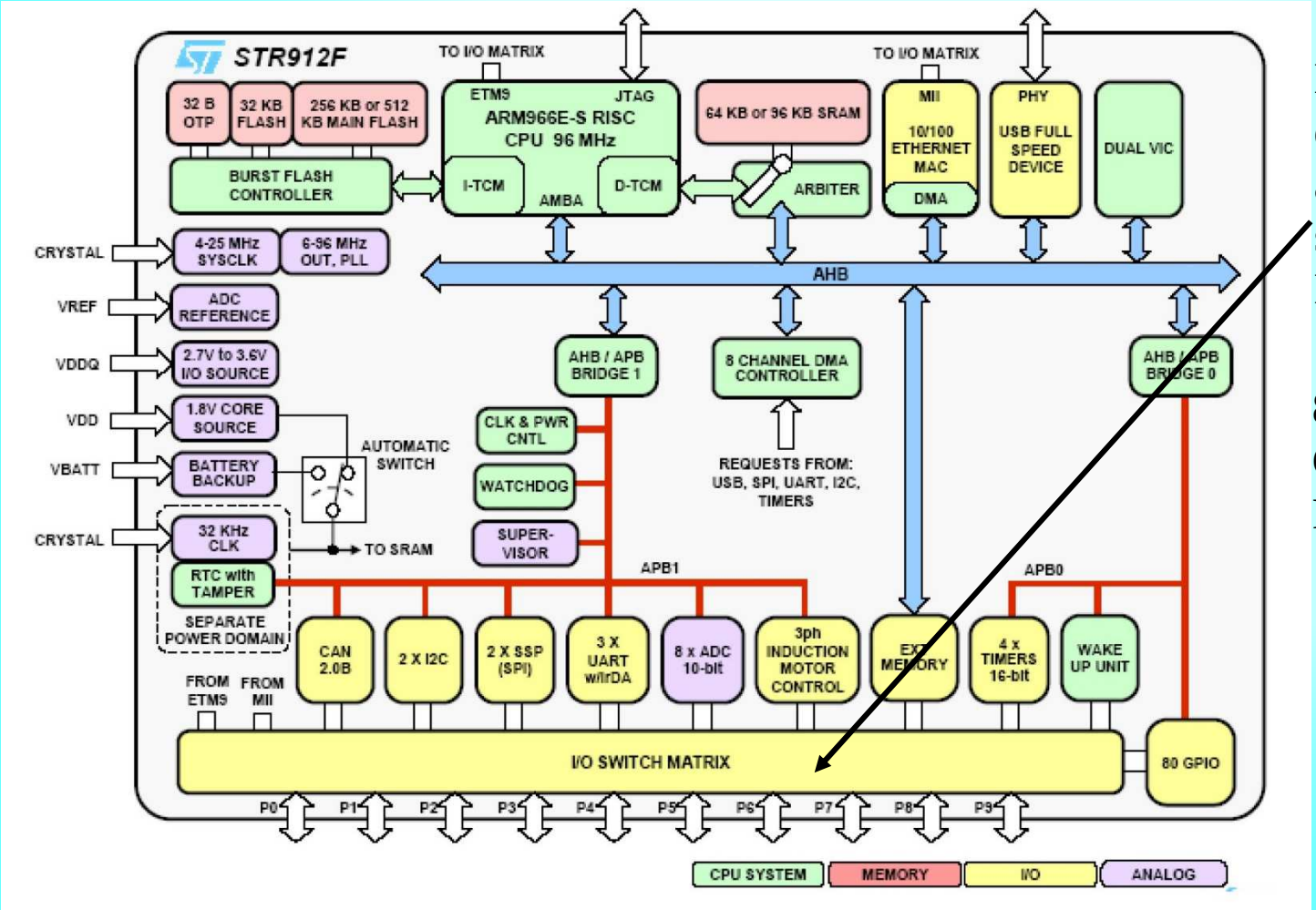
Intégration mémoire VIVE SRAM

Microcontrôleur



Processeur utilisé STR912
(ST Microelectronic)

Architecture Interne



Le STR9 a 80 lignes d'entrées sorties à usage général répartie sur 9 Ports partagés ave D'autres périphériques

8 lignes entrées sorties GPIO
Par port
configuration en sortie push-pull ou collecteur ouvert

Processeur utilisé STR912
(ST Microelectronic)

Architecture Interne

Les ports partagés

Peripheral	# No of Unit	Port Assignment	IO Mode	Peripheral	# No of Unit	Port Assignment	IO Mode
ADC	8 chann-els	P4	Always Connected	Motor Control	1	P6	Alt Out
CAN	1	P1, P3, P5	Alt In Alt out	SSP	2	P2, P5	Alt In Alt Out
ETM	1	P0,P2,P4,P5, P6, P7	Alt In Alt Out	Timers	4	P0, P4, P6, P7	Alt In Alt Out
Ethernet MAC	1	P0, P1, P5	Always Connected	UART	3	P1, P2, P3, P5, P6, P7	Alt In Alt Out
EMI	Mux	P8, P9, P7	P7 – Alt Out	USB	1	D+/D- Ext clk – P3	Dedicated pins
	Non-mux	P8, P9, P7	P7 – Alt Out	External Interrupt	30	P3, P5, P6, P7	Always Connected
Chip Select	4	P0, P5, P7	Alt Out	External DMA Req	2	P3	Always Connected
I2C	2	P0, P1, P2	Alt In Alt Out				

ADC : sur port N°4

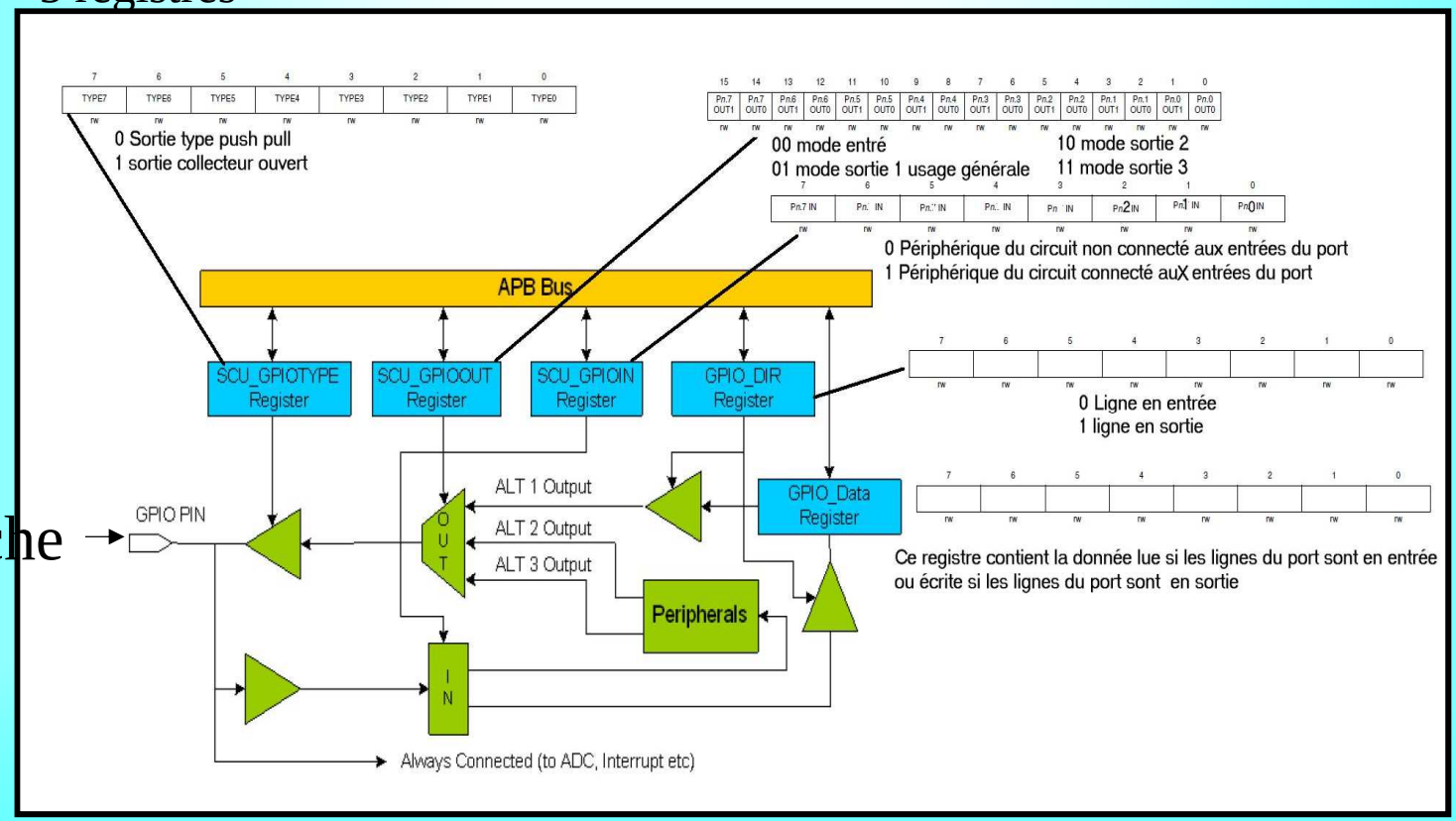
Processeur utilisé STR912
(ST Microelectronic)

Architecture Interne

Programmation des broches d'entrées sorties

Pour chacun des ports entrée sorties
5 registres

1 broche



Processeur utilisé STR912
(ST Microelectronic)

Architecture Interne

Programmation des broches d'entrées sorties

Type d'entrée sorties que l'on peut avoir sur une ligne des ports

Pin I/O Alternative Modes	*Input (Default)*	*Input - Alt*	*Output -* mode 1	*Output -* mode 2	*Output -* mode 3	*Input Always Connected*
Peripheral Function Supported	GPIO Input	Timer Inputs (Input Capture)	GPIO Output	Timer Outputs (Output Compare)	ETM Outputs	ADC Inputs

Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

Le port 4 a un registre mode analogique dédié qui connecte les broches externes aux différents canaux du CAN SCU_GPIOANA.

ADC : sur port N°4

SCU_GPIOINn SCU_GPIOUTn à 0
n : numéro du bit

GPIO analog mode register (SCU_GPIOANA)

Address Offset: BCh

Reset value: 0000 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								P4.7A	P4.6A	P4.5A	P4.4A	P4.3A	P4.2A	P4.1A	P4.0A
								rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:8	Reserved, always read as 0.
Bits 7:0	**P4[7:0]A:** *GPIO Port 4 Analog Control bits* These bits are set and cleared by software to configure the corresponding GPIO port 4 pin in analog mode. When you use analog mode, clear the corresponding bits in the SCU_GPIOIN*n* and SCU_GPIOUT*n* registers. 0: Analog mode off 1: Analog mode on See also *Section 1 on page 3*

Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

Le port 4 a un registre mode analogique dédié qui connecte les broches externes aux différents canaux du CAN SCU_GPIOANA.

ADC : sur port N°4

SCU_GPIOINn SCU_GPIOUTn à 0
n : numéro du bit

GPIO analog mode register (SCU_GPIOANA)

Address Offset: BCh

Reset value: 0000 0000h

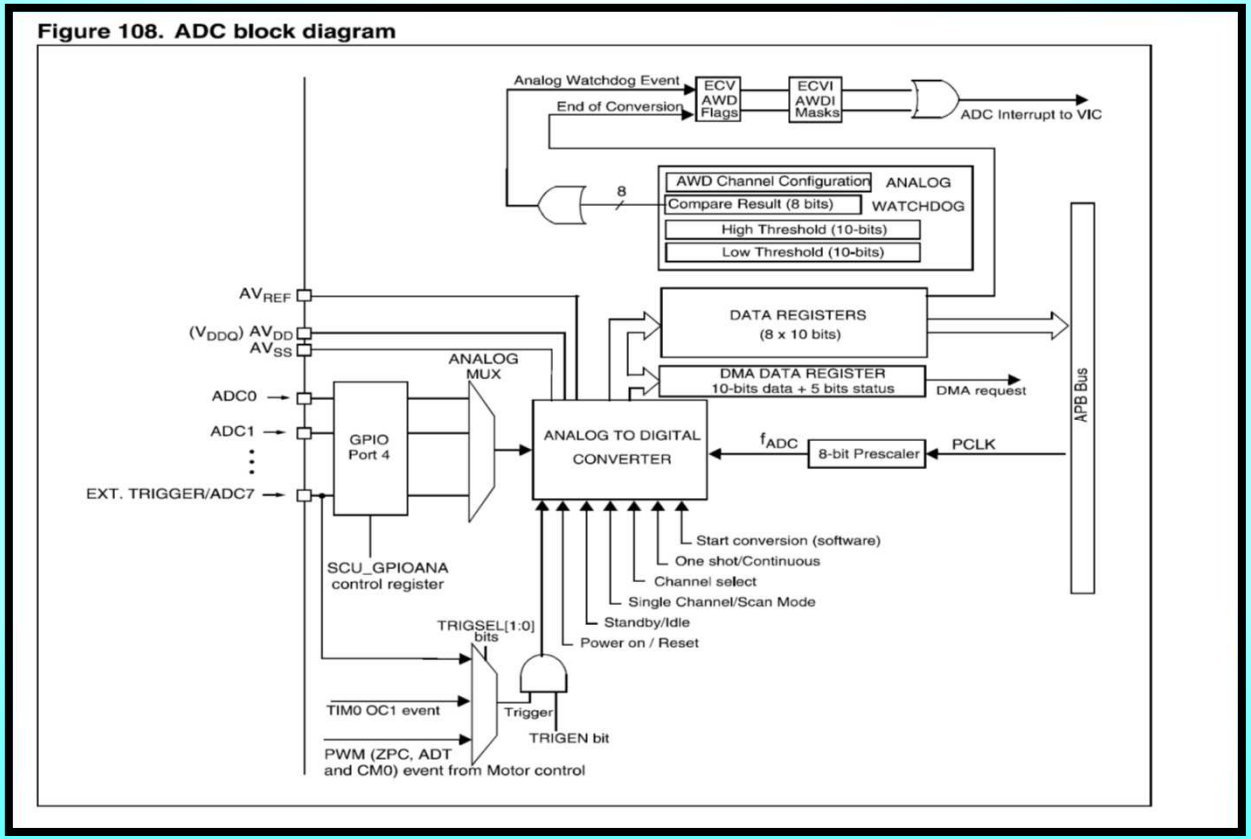
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								P4.7A	P4.6A	P4.5A	P4.4A	P4.3A	P4.2A	P4.1A	P4.0A
								rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:8	Reserved, always read as 0.
Bits 7:0	**P4[7:0]A:** *GPIO Port 4 Analog Control bits* These bits are set and cleared by software to configure the corresponding GPIO port 4 pin in analog mode. When you use analog mode, clear the corresponding bits in the SCU_GPIOIN*n* and SCU_GPIOUT*n* registers. 0: Analog mode off 1: Analog mode on See also *Section 1 on page 3*

Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

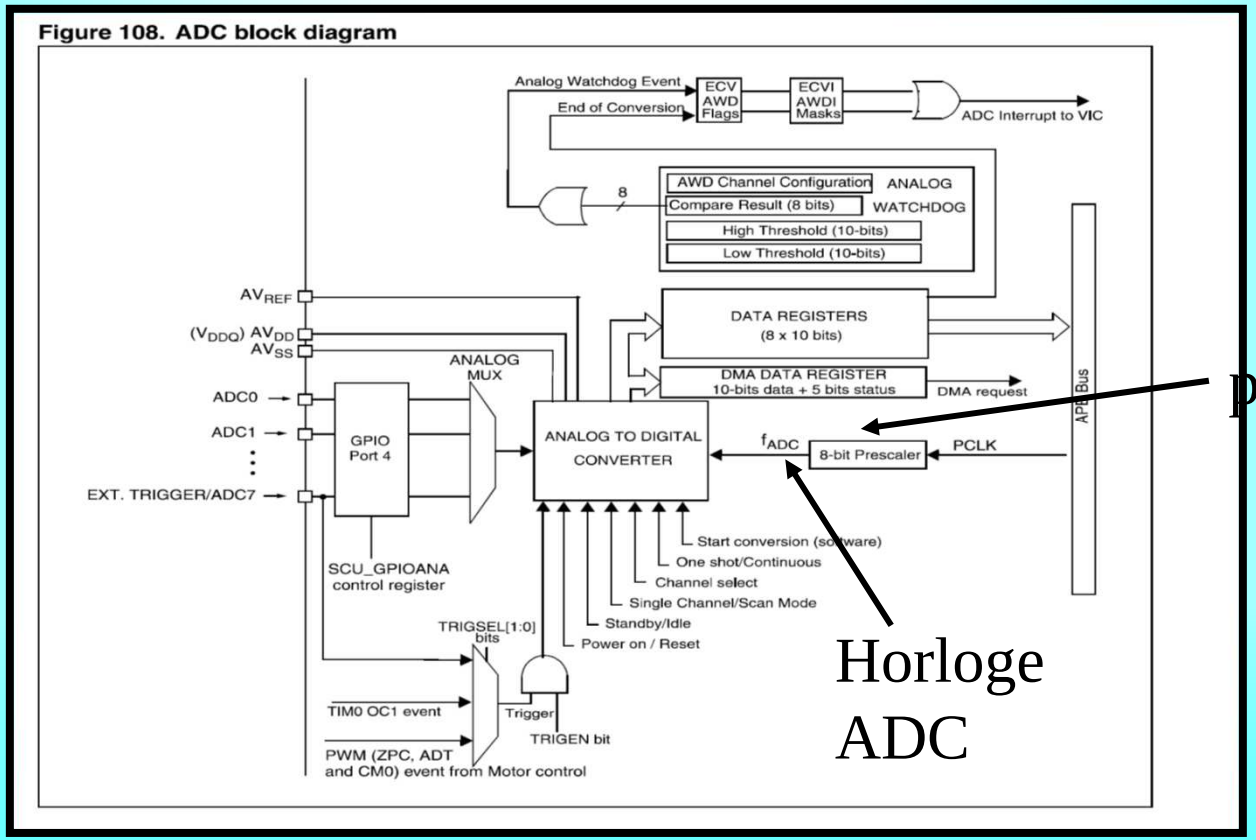
numérise jusqu'à 8 canaux analogiques
résolution : 10 bits



Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

numérise jusqu'à 8 canaux analogiques
résolution : 10 bits



prédiviseur
A
programmer

Horloge
ADC

Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

Le registre de contrôle

ADC control register (ADC_CR)

Address offset: 00h
Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECV	AWD	Reserved			ECVI	AWDI	SC[2:0]			SCE	CONT	STB	res.	POR	STR
rc_w1	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16	Reserved, forced by hardware to 0
Bit 15	**ECV:** *End of conversion flag* This bit is set by hardware and cleared by software writing 1. 0: No end of conversion event 1: End of conversion. You can read the ADC_DRx registers to retrieve the result An interrupt request is generated if ECVI = 1.
Bit 14	**AWD:** *Analog Watchdog flag* 0: No analog watchdog event 1: An analog watchdog event occurred. You can read the ADC_CRR register to determine the result for each channel. An interrupt request is generated if AWDI = 1.
Bits 13:12	Reserved, forced by hardware to 0
Bit 11	Reserved, must be kept at reset value 0
Bit 10	**ECVI:** *End of conversion interrupt enable* 0: ECV interrupt disabled 1: ECV interrupt enabled
Bit 9	**AWDI:** *Analog watchdog interrupt enable* 0: AWD interrupt disabled 1: AWD interrupt enabled
Bits 8:6	**SC[2:0]:** *Selected channel to be converted* These bits are written by software to select the channel to be converted. The selection applies only when Scan mode is disabled (SCE=0). The channel to be converted must also be configured as active in the ADC_CCR register. 000: Channel 0 001: Channel 1 ... 111: Channel 7
Bit 5	**SCE:** *Scan mode enable* This bit is set and cleared by software. 0: Single channel mode. The channel selected by the SC[2:0] bits is enabled 1: Scan mode. All channels configured as active in the ADC_CCR register are converted.
Bit 4	**CONT:** *Continuous mode enable* This bit is set and cleared by software. 0: One shot mode: if SCE = 0 the channel selected by the SC[2:0] bits is converted once. The STR bit is cleared automatically and the ECV bit is set at the end of conversion. If SCE = 1 all channels are converted once. The STR bit is cleared automatically and the ECV bit is set at the end of conversion. 1: Continuous mode, if SCE = 0 the channel selected by the SC[2:0] is converted continuously. If SCE = 1 all channels are converted continuously. The STR bit must be cleared by software to stop conversion.
Bit 3	**STB:** *Standby mode enable* This bit is set and cleared by software. 0: Idle mode. The analog block is kept powered on 1: Standby mode enabled. The analog block is put in low power mode ***Note:*** When STB is cleared, the first conversion can start after 15 µs.
Bit 2	Reserved, must be kept at reset value 0.
Bit 1	**POR:** *Power on/ Reset mode* This bit is set and cleared by software. 0: Reset mode. The analog block is switched off, all registers are reset. Write access to all registers disabled except POR bit. 1: Power on mode. ADC digital block is running. Analog block in Idle mode or Standby mode depending on the STB bit. ***Note:*** When POR is set, the first conversion can start only after $t_{POR(ADC)}$
Bit 0	**STR:** *Start Conversion* This bit is set and cleared by software. 0: Stop Conversion The ADC returns to Idle state at the next clock pulse. 1: Start conversion The first conversion starts after up 3 x 16 ADC clock cycles (synchronously with analog block).

L'ADC peut générer trois requêtes d'interruption masquables :

- Fin de conversion
- Chien de garde analogique
- Mémoire DMA saturée

Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

Le registre de configuration des canaux

2 bits pour un canal
Canal 0

Channel configuration register (ADC_CCR)

Address offset: 04h
Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC7[1:0]		CC6[1:0]		CC5[1:0]		CC4[1:0]		CC3[1:0]		CC2[1:0]		CC1[1:0]		CC0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16	Reserved, forced by hardware to 0
Bits 15:0	**CCx[1:0]:** *Channel x Configuration (x = 7:0)* These bits are written by software to configure the corresponding ADC input channel. 00: No A/D conversion or watchdog feature on channel x 01: Active for A/D conversion, analog watchdog event configured to trigger when the converted result on channel x is greater than the low threshold (CDATA > LT). 10: Active for A/D conversion, analog watchdog configured to trigger when the converted result on channel x is less than the high threshold (CDATA < HT). 11: Active for A/D Conversion without watchdog feature on channel x

Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

Le registre de donnée contient le résultat de la conversion

ADC data register (ADC_DRx)

x numéro du canal

There are eight ADC data registers (x can be a value from 0 to 7)
Address offset: 14h...30h
Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OV	Reserved					CDATA[9:0]									
r						r	r	r	r	r	r	r	r	r	r

Bits 31:16	Reserved, forced by hardware to 0
Bit 15	**OV:** *Channel x Overflow status* This bit is updated by hardware after each conversion. 0: No overflow on this channel 1: A conversion overflow occurred on this channel
Bits 14:10	Reserved, forced by hardware to 0
Bits 9:0	**CDATA[9:0]:** *Channel x Converted Data* The conversion results for the eight available channels are loaded into the eight different data registers following conversion of the corresponding analog input.

Résultat
Sur 10bits

Processeur utilisé STR912
(ST Microelectronic)

Le Convertisseur analogique numérique

Le registre Prédiviseur détermine la fréquence du CAN fADC

ADC prescaler register (ADC_PRS)

Address offset: 34h
Reset value: 00FFh

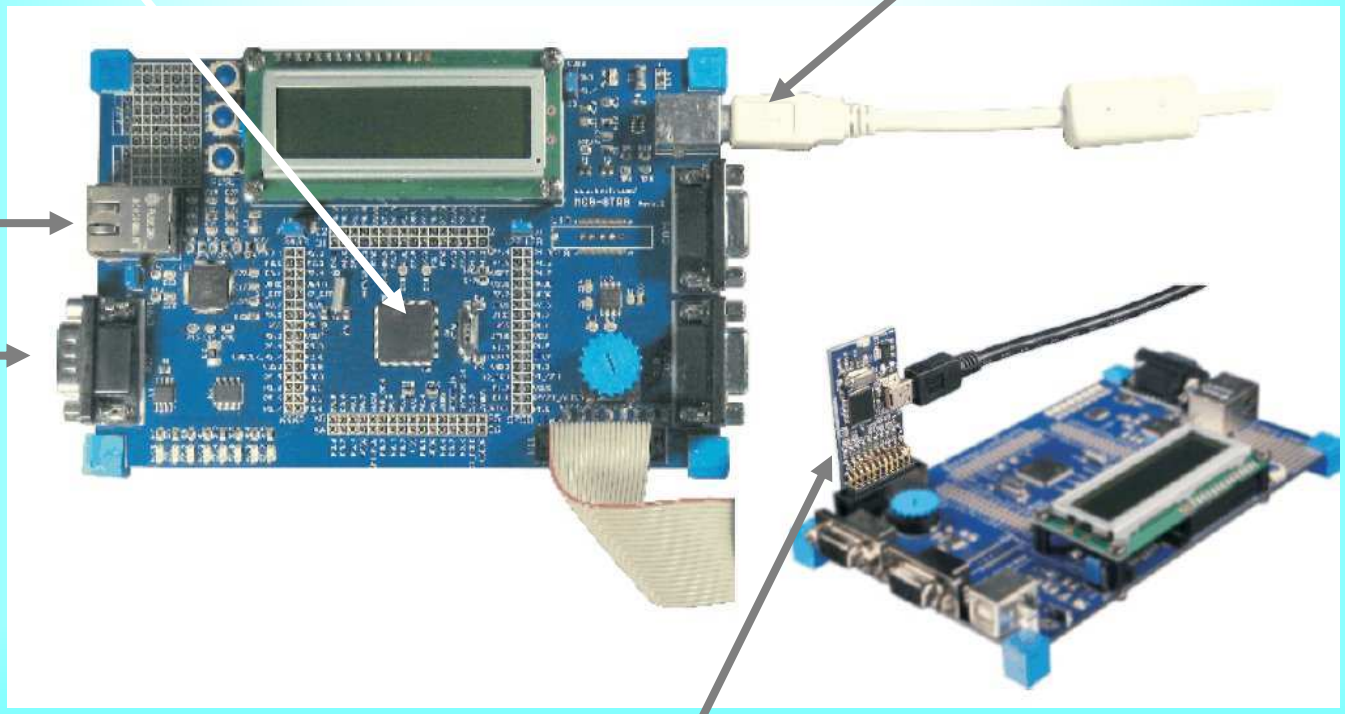
7	6	5	4	3	2	1	0
PRS[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:8	Reserved, forced by hardware to 0
Bits 7:0	**PRS[7:0]:** *ADC Prescaler* These bits are written by software to define the ADC clock prescaling factor. 00h: f_{ADC}=PCLK 01h: f_{ADC}=PCLK 02h: f_{ADC}=PCLK/2 .. FFh: f_{ADC}=PCLK/255

Processeur utilisé STR912
(ST Microelectronic)

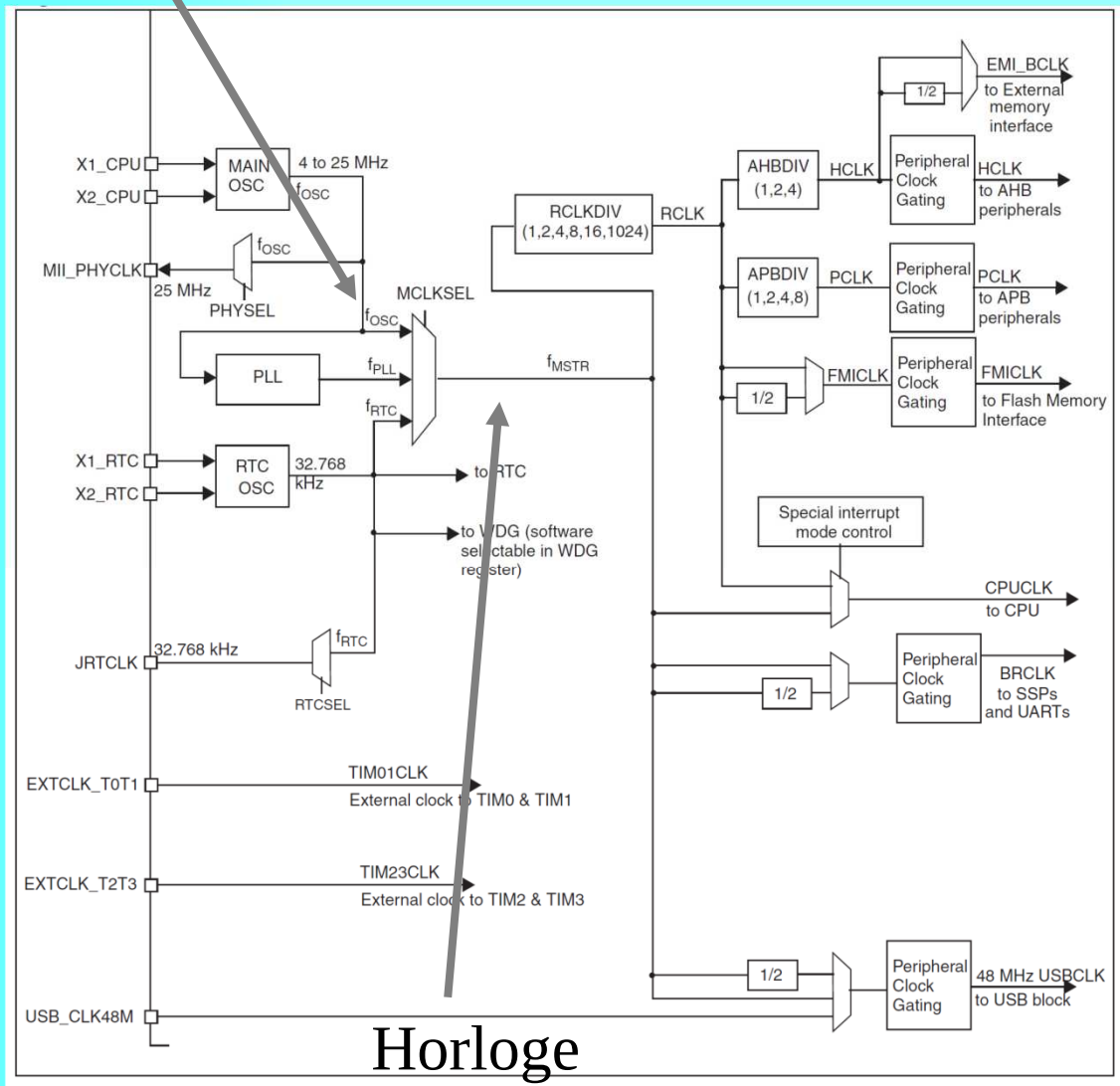
La carte de développement est une carte de la société Keil **MCBSTR9**

Architecture Kit de développement



Processeur STR912
(ST Microelectronic)
Gestion des Horloges

FOSCmax=25MHz



Horloge Principale FMSTR

Si FPLL=FMSTR

$$FPLL = \frac{2*N*FOSC}{M*2^{P}}$$

$$1MHz \leq \frac{FOSC}{(M)} \leq 2MHz$$

$$200MHz \leq \frac{2 \times N \times FOSC}{(M)} \leq 622MHz$$

Sous la suite logicielle Micro-vision 4

Processeur STR912
(ST Microelectronic)
Gestion des Horloges

Si FMSTR=FPLL

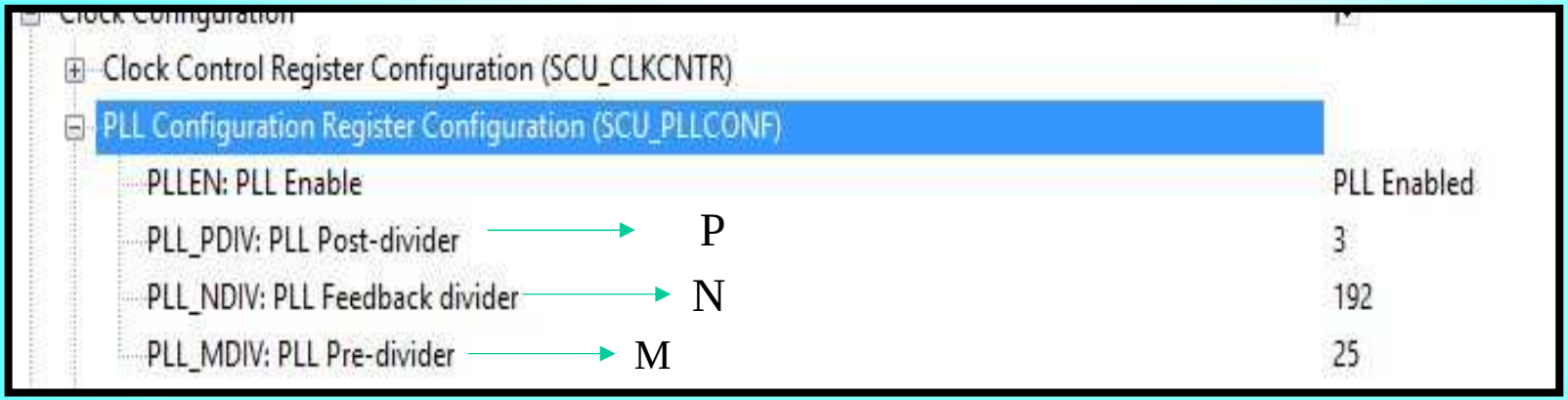
$$FPLL = \frac{2*N*FOSC}{M*2^{P}}$$

FOSC=25MHz

$$1MHz \leq \frac{FOSC}{(M)} \leq 2MHz$$

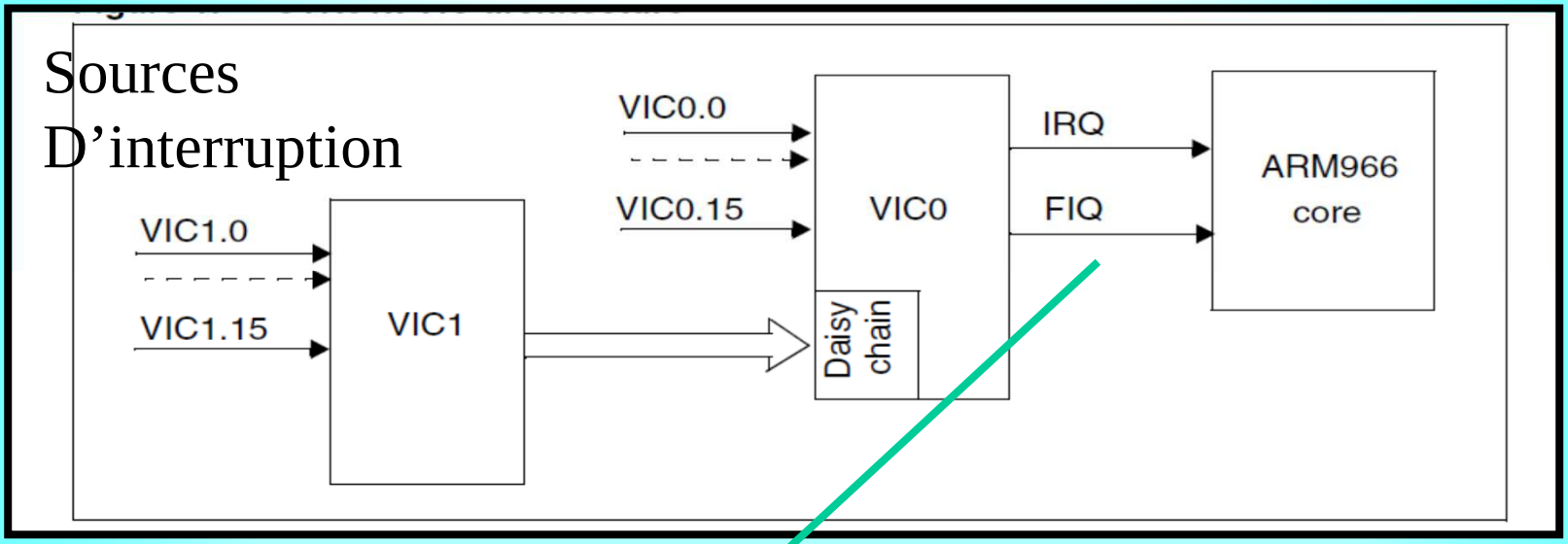
$$200MHz \leq \frac{2 \times N \times FOSC}{(M)} \leq 622MHz$$

Sous la suite logicielle
Micro-vision 4 Configuration de la PLL



Processeur STR912
(ST Microelectronic)
Gestion des Interruption

32 Interruptions émanant des périphériques vers le cœur ARM9
16 Interruptions VIC0 (Contrôleur de vecteur d'interruption)
16 Interruptions VIC1 (Contrôleur de vecteur d'interruption)



2 types d'interruptions

FIQ (Fast interrupt Request)
Interruption rapide et prioritaire

IRQ (interrupt Request)
Interruption usage normal

Processeur STR912
(ST Microelectronic)
Les sources d'interruption

16 Canaux d'interruption venant des périphériques du microcontrôleur

Table 13. VIC interrupt channels

VIC input channel	Logic block	Interrupt source
VIC0.0	Watchdog	Timeout in WDG mode, End of Count in Counter Mode
VIC0.1		Software interrupt
VIC0.2	CPU Core	Debug Receive Command
VIC0.3	CPU Core	Debug Transmit Command
VIC0.4	TIM Timer 0	Logic OR of ICI0_0, ICI0_1, OCI0_0, OCI0_1, Timer overflow
VIC0.5	TIM Timer 1	Logic OR of ICI1_0, ICI1_1, OCI1_0, OCI1_1, Timer overflow
VIC0.6	TIM Timer 2	Logic OR of ICI2_0, ICI2_1, OCI2_0, OCI2_1, Timer overflow
VIC0.7	TIM Timer 3	Logic OR of ICI3_0, ICI3_1, OCI3_0, OCI3_1, Timer overflow
VIC0.8	USB	Logic OR of high priority USB interrupts
VIC0.9	USB	Logic OR of low priority USB interrupts
VIC0.10	SCU	Logic OR of all interrupts from System Control Unit (SCU) except Early warning
VIC0.11	Ethernet MAC	Logic OR of Ethernet MAC interrupts via its own dedicated DMA channel.
VIC0.12	DMA	Logic OR of interrupts from each of the 8 individual DMA channels
VIC0.13	CAN	Logic OR of all CAN interface interrupt sources
VIC0.14	MC	Logic OR of 8 Induction Motor Control Unit interrupts
VIC0.15	ADC	End of A/D conversion or analog watchdog interrupt

Table 13. VIC interrupt channels (continued)

VIC input channel	Logic block	Interrupt source
VIC1.0	UART0	Logic OR of 5 interrupts from UART channel 0
VIC1.1	UART1	Logic OR of 5 interrupts from UART channel 1
VIC1.2	UART2	Logic OR of 5 interrupts from UART channel 2
VIC1.3	I2C0	Logic OR of transmit, receive, and error interrupts of I2C channel 0
VIC1.4	I2C1	Logic OR of transmit, receive, and error interrupts of I2C channel 1
VIC1.5	SSP0	Logic OR of all interrupts from SSP0
VIC1.6	SSP1	Logic OR of all interrupts from SSP1
VIC1.7	SCU	LVD early warning interrupt (Brownout)
VIC1.8	RTC	Logic OR of Alarm, Tamper, or Periodic Timer interrupts
VIC1.9	WIU (all)	Logic OR of all 32 inputs of Wakeup unit (30 pins, RTC, and USB Resume)
VIC1.10	WIU Group 0	One of 8 interrupt sources: RTC, USB Resume, pins P3.2 to P3.7 selected by SCU_WKUPSEL register
VIC1.11	WIU Group 1	One of 8 interrupt sources from pins P5.0 to P5.7 selected by SCU_WKUPSEL register
VIC1.12	WIU Group 2	One of 8 interrupt sources from pins P6.0 to P6.7 selected by SCU_WKUPSEL register
VIC1.13	WIU Group 3	One of 8 interrupt sources from pins P7.0 to P7.7 selected by SCU_WKUPSEL register
VIC1.14	USB	USB Bus Resume Wakeup (also input to wakeup unit)
VIC1.15	PFQ-BC	Special use of interrupts from Prefetch Queue and Branch Cache

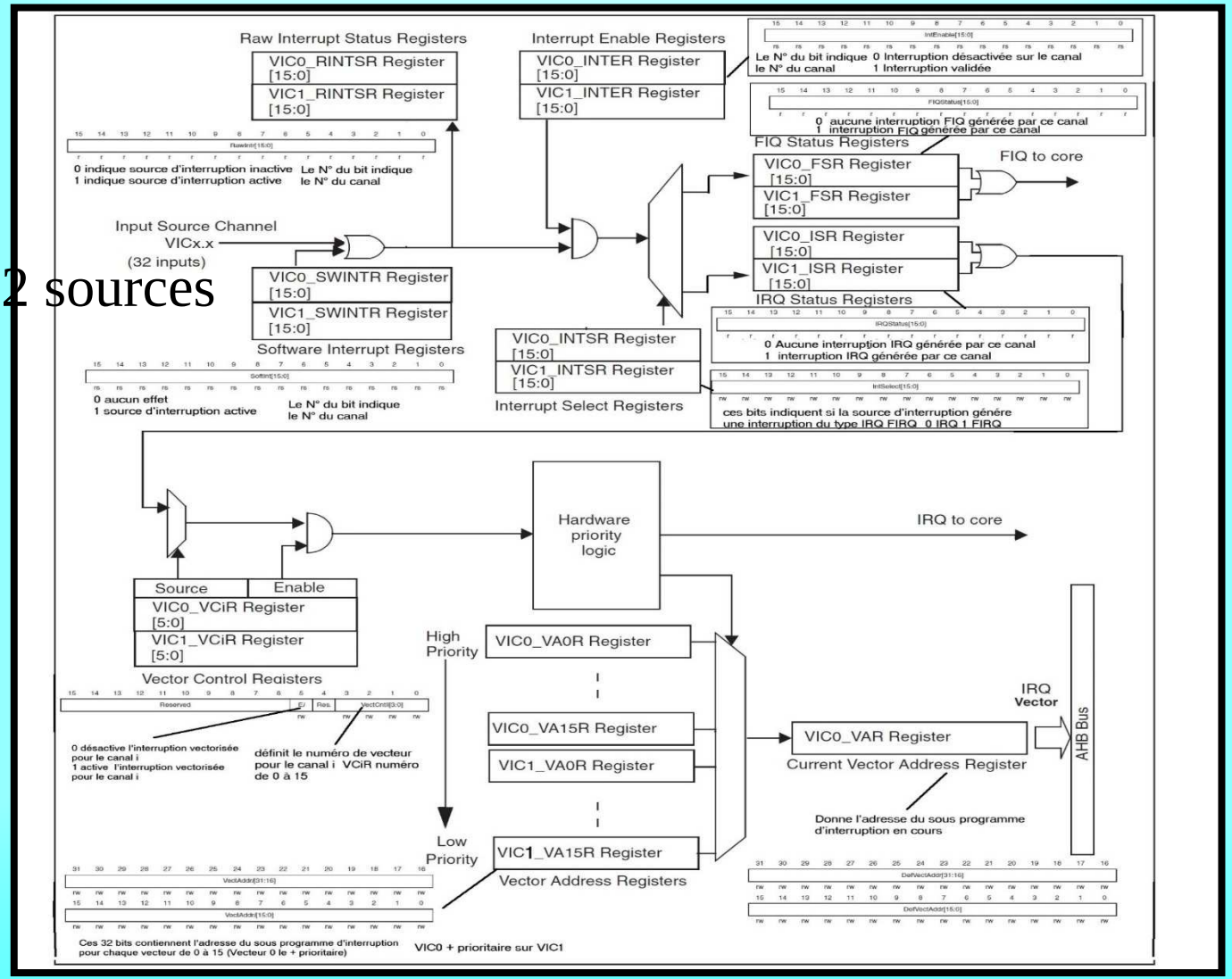
Processeur STR912 (ST Microelectronic)

Les sources d'interruption

Les 32 sources d'interruption venant des périphériques du microcontrôleur sont gérées de la manière suivante:

VIC0 & VIC1

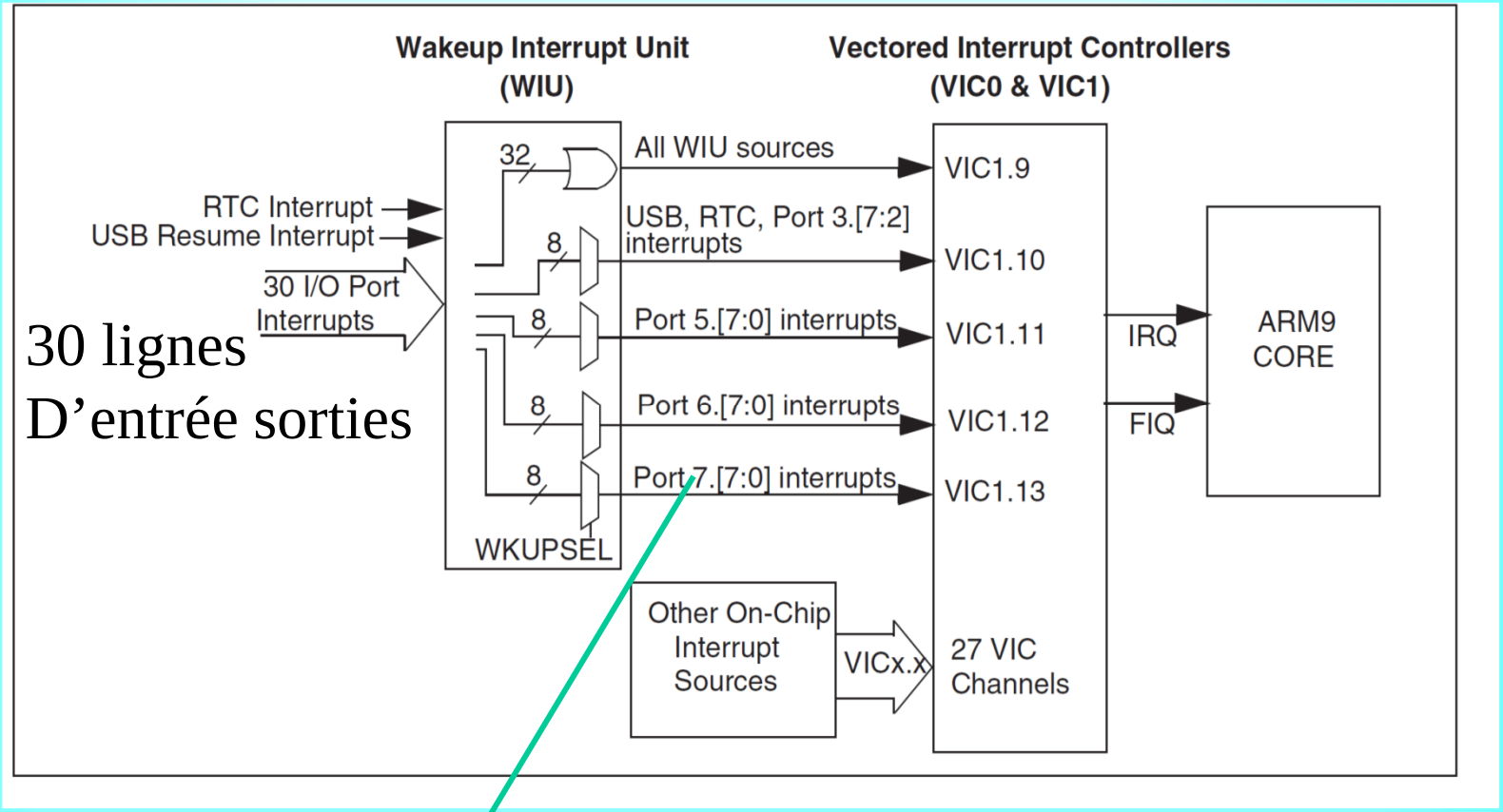
32 sources



Processeur STR912 (ST Microelectronic)

Les sources d'interruption

Le module **WAKE-UP/ Interrupt Unit (WIU)** Gère entre autre les interruptions pour les broches d'entrées sorties du microcontrôleur



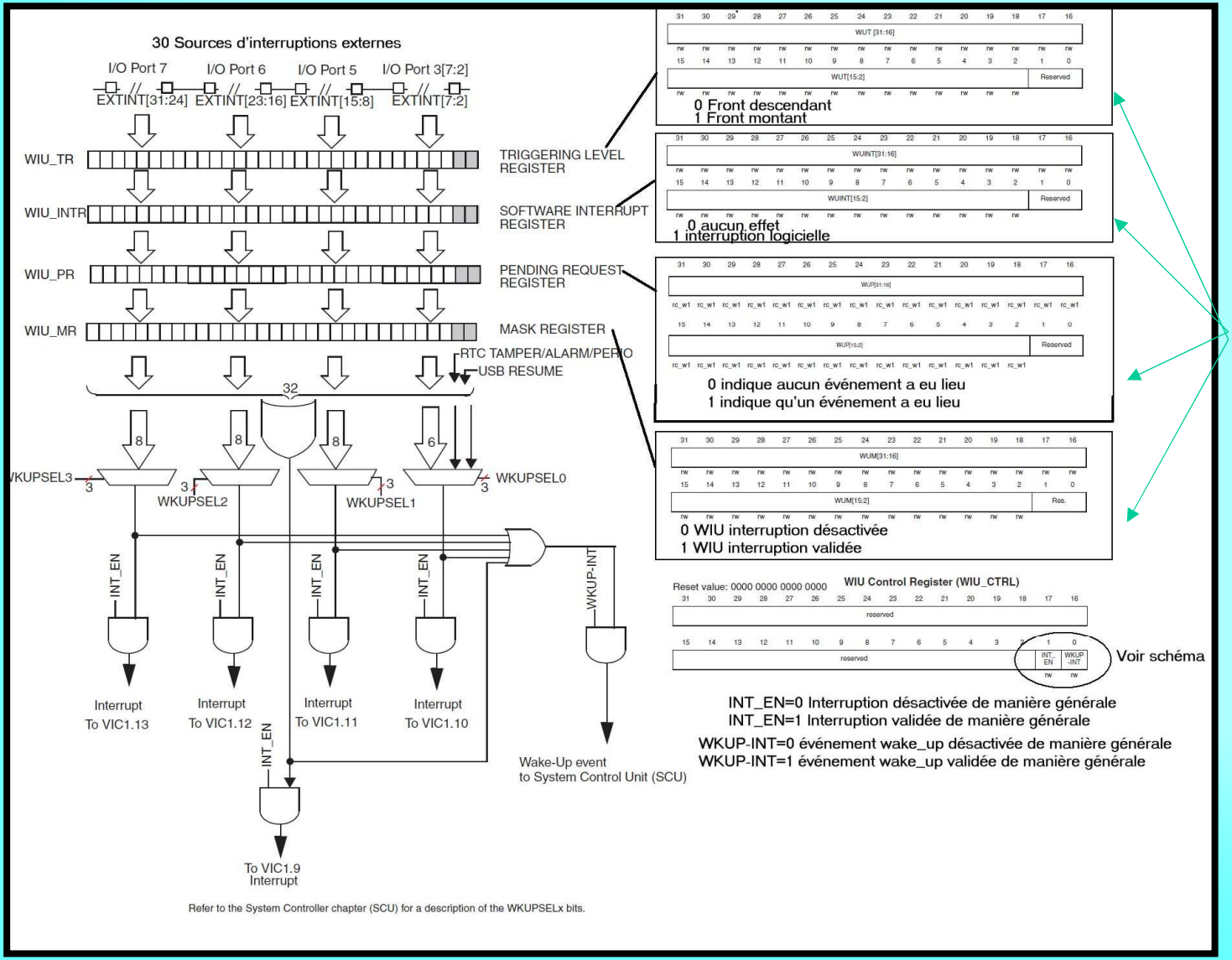
30 lignes
D'entrée sorties

8 Sources d'interruption Potentielles sur le PORT7 → Sur le canal N°13 VIC1

Processeur STR912 (ST Microelectronic)

Les sources d'interruption Registres du WIU

Le module **WAKE-UP/ Interrupt Unit (WIU)** Gère entre autre les interruptions pour les broches d'entrées sorties du microcontrôleur



Registre à Programmer Ou à lire