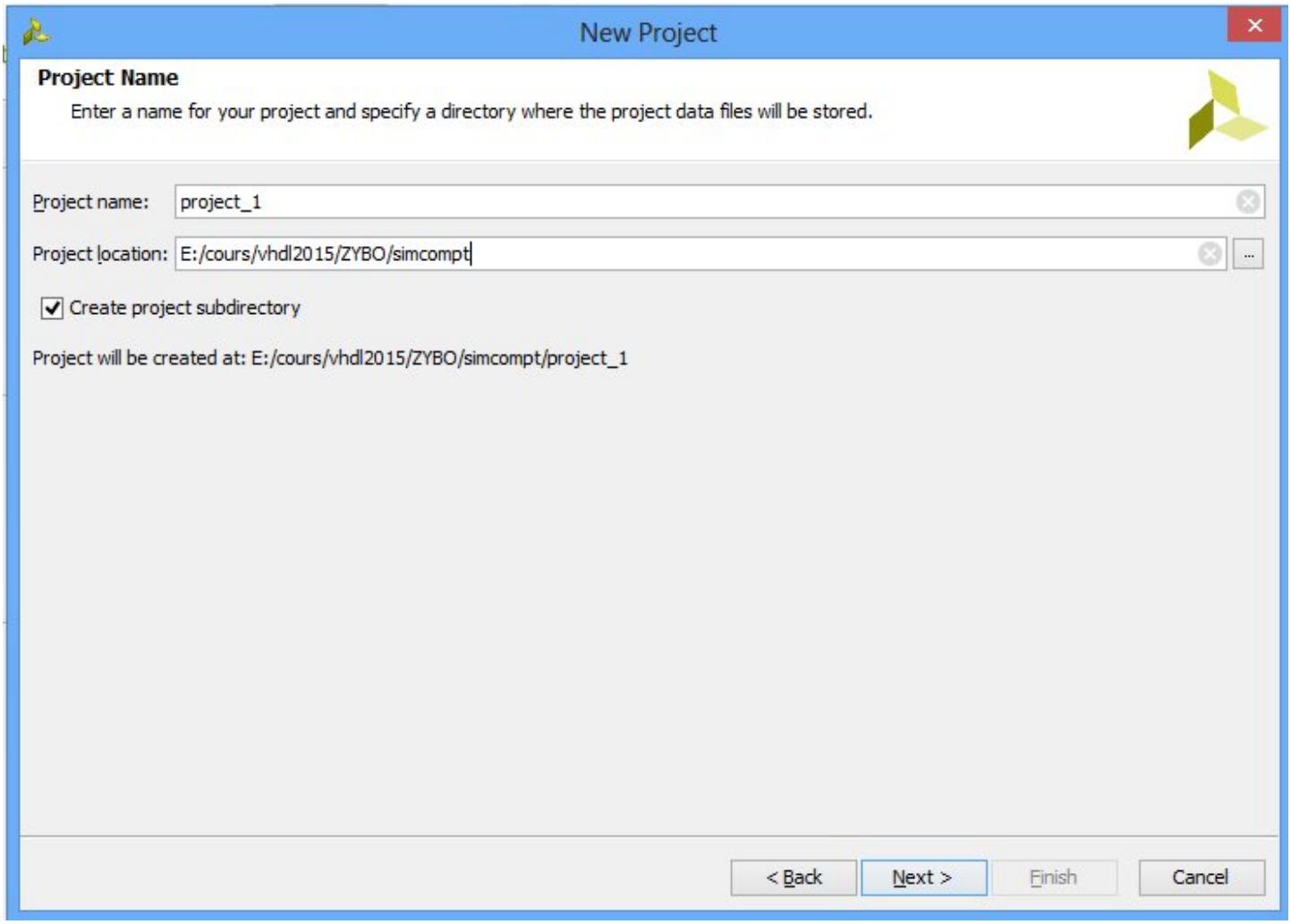
Simulation avec modelsim

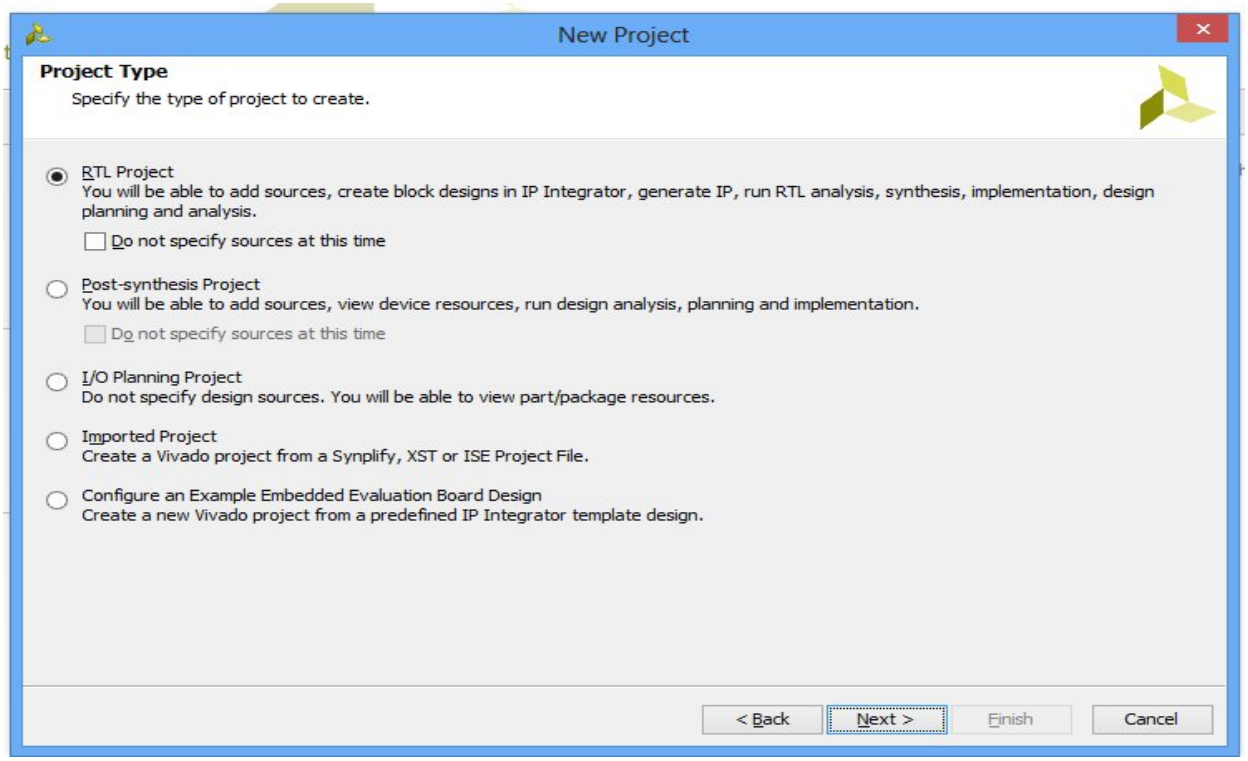
Cette séance nous permettra de s'initier aux outils de développement Vivado et notamment l'outil de simulation vivado simulation ou Modelsim.
L'exemple choisi restera anecdotique car celui-ci sera un simple compteur à modéliser en code VHDL.

Mise en place matériel

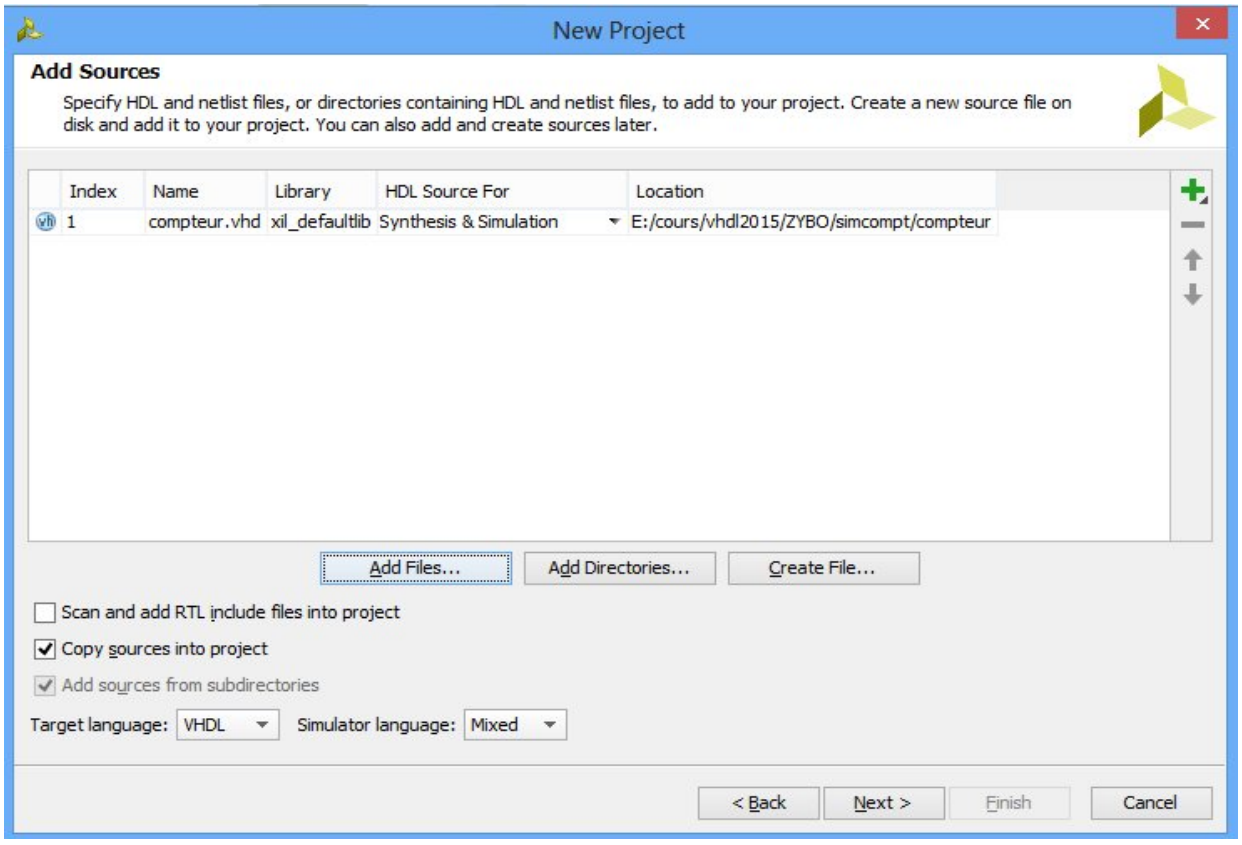
Créez un nouveau projet sur vivado



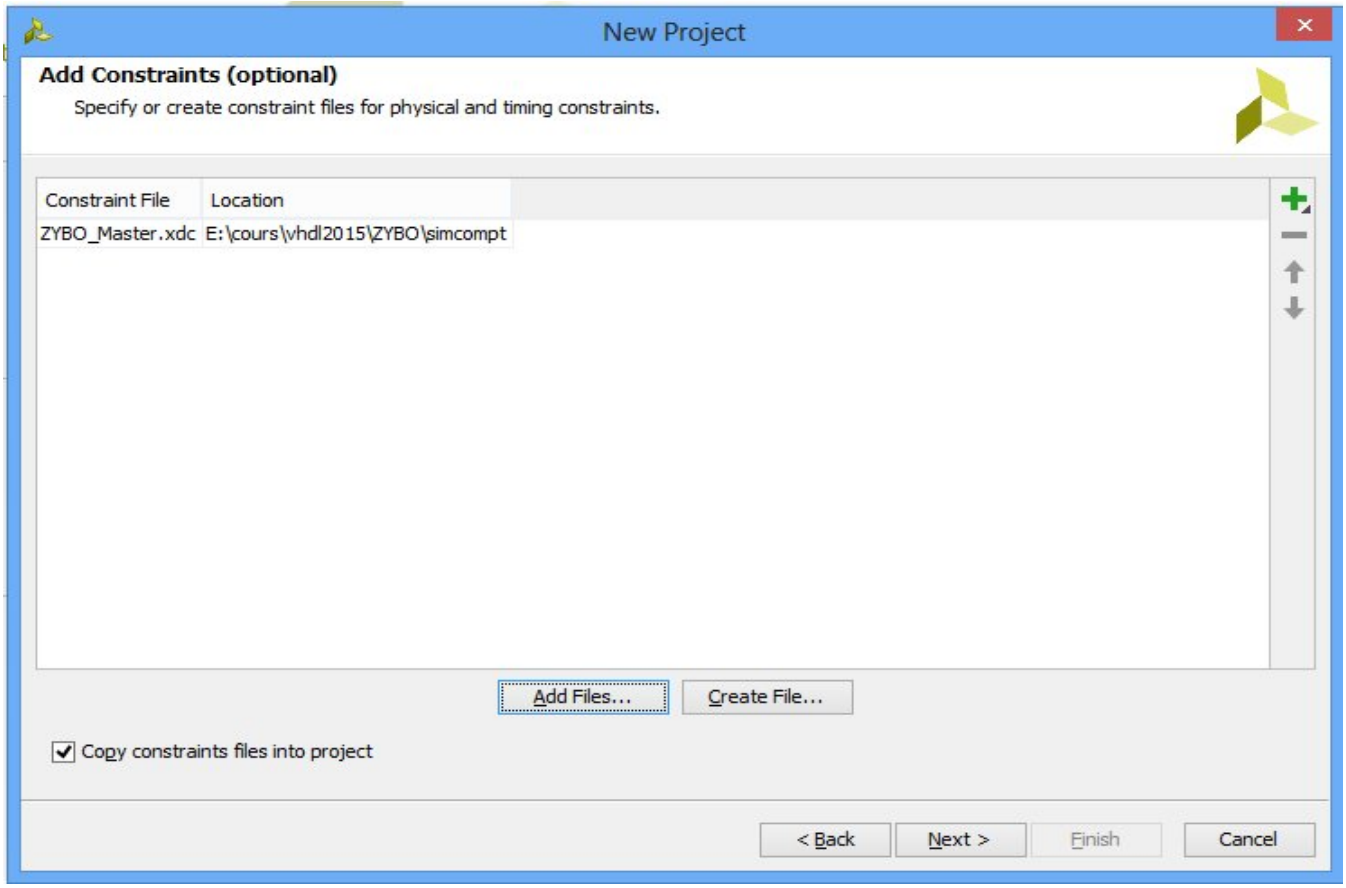
Du type RTL

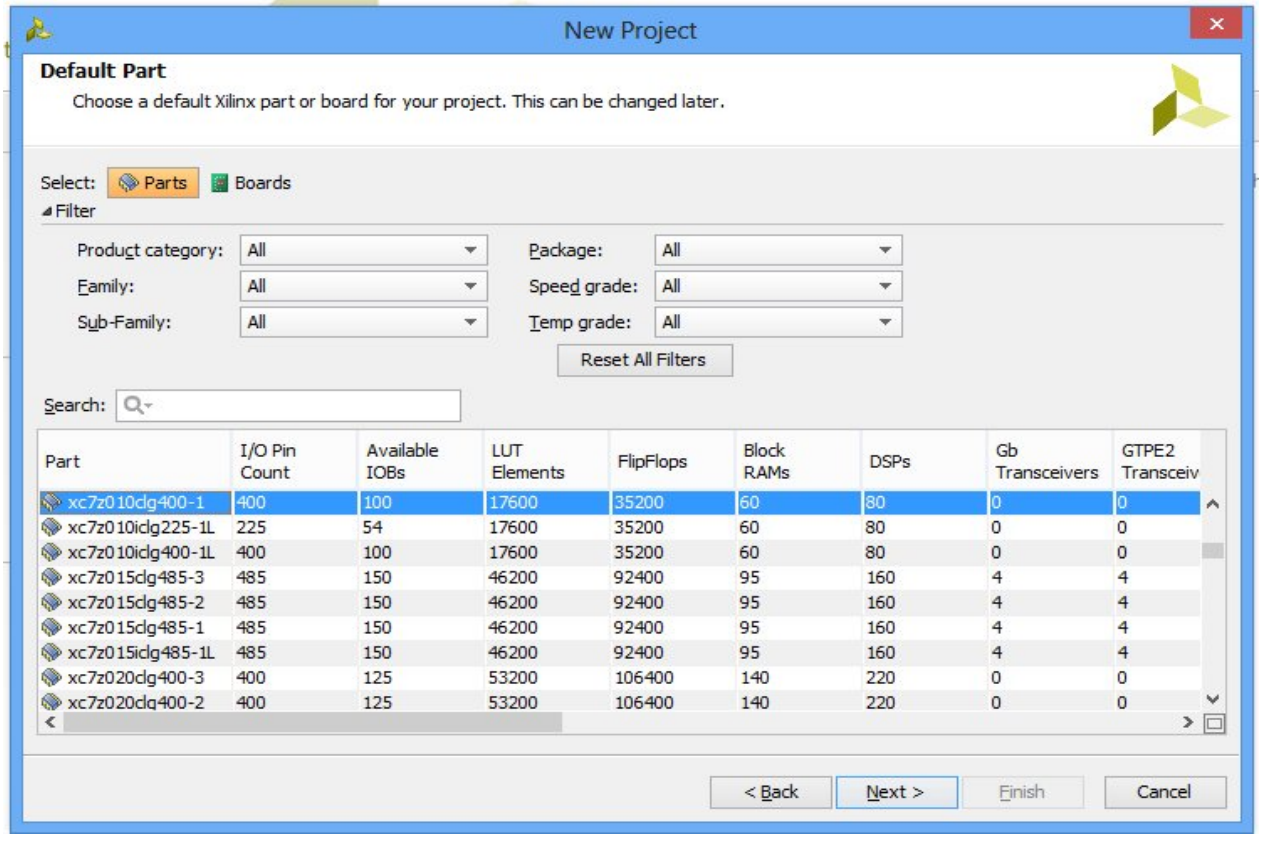


Additionnez le code VHDL de notre compteur

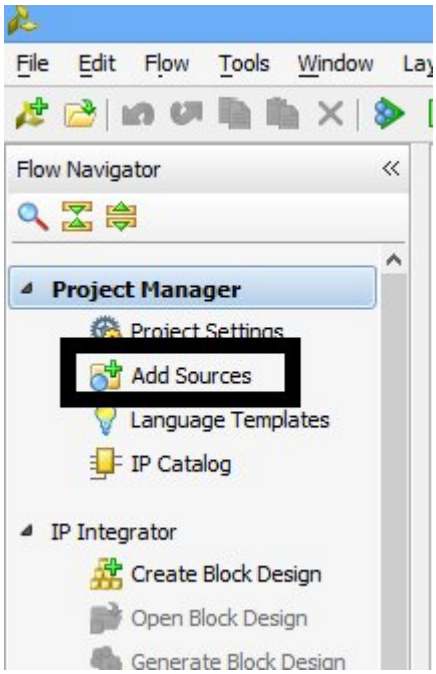


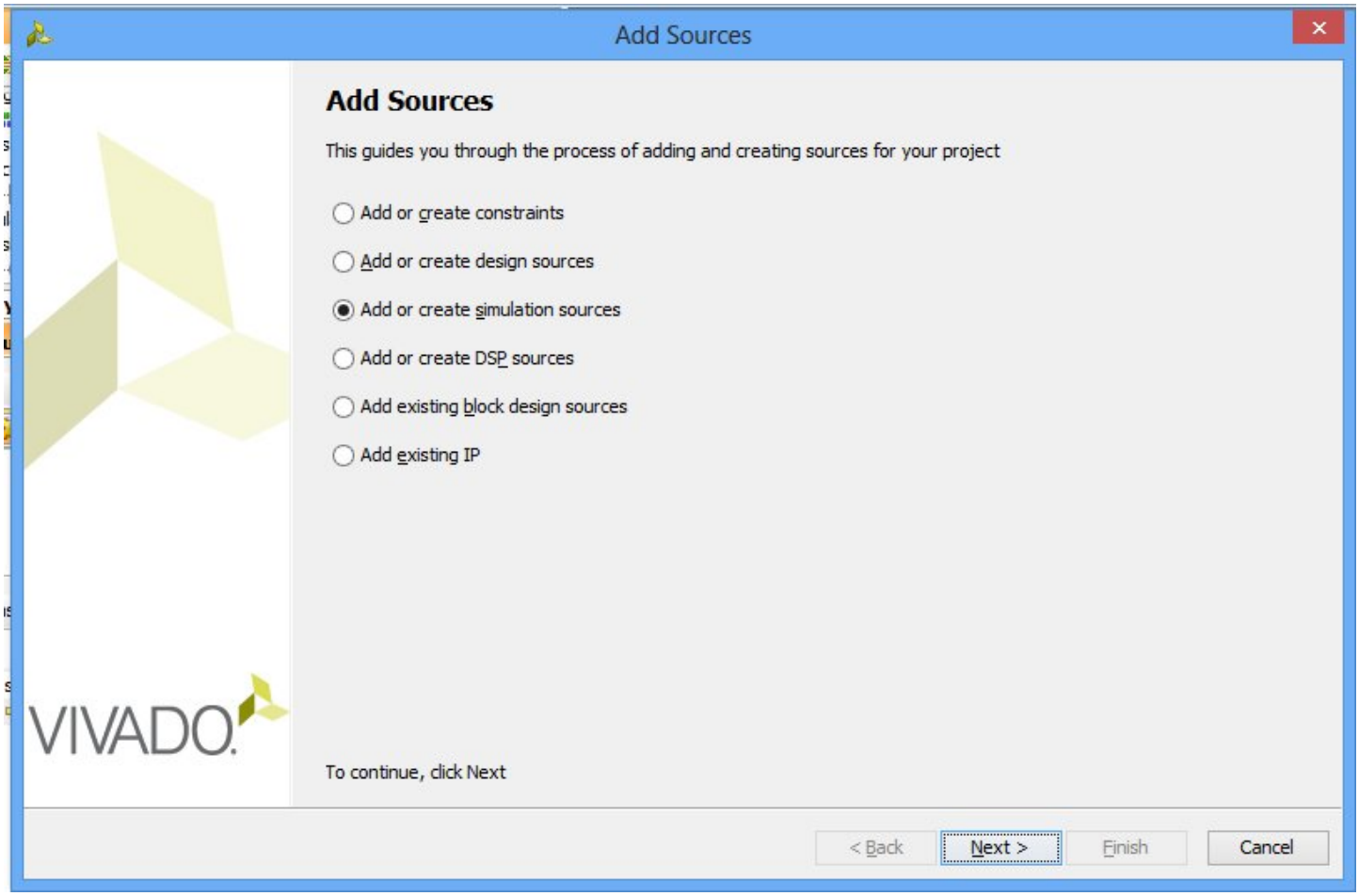
Associez le fichier de contrainte pour la carte zybo



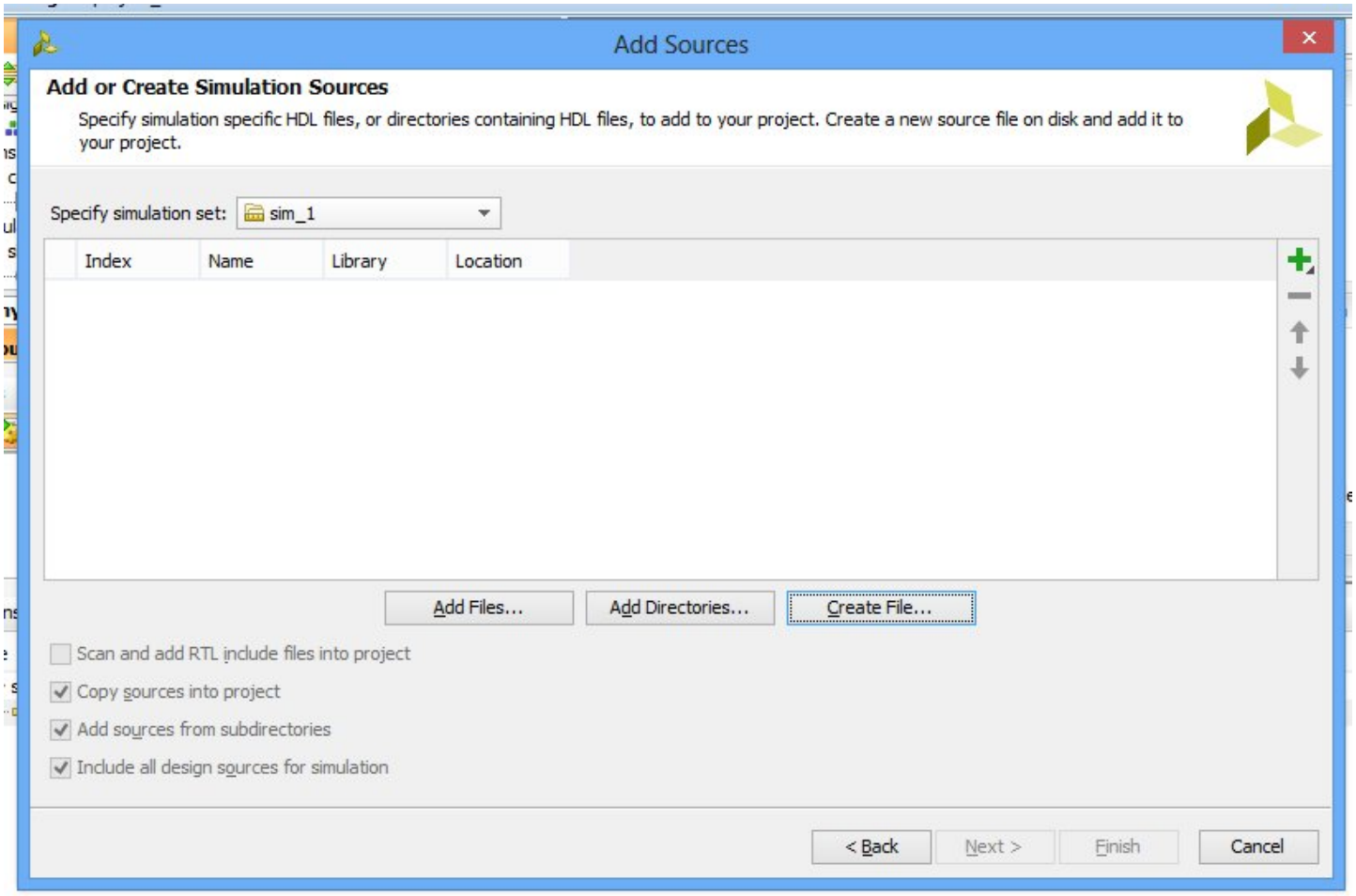


On va créer un fichier de simulation du type testbench

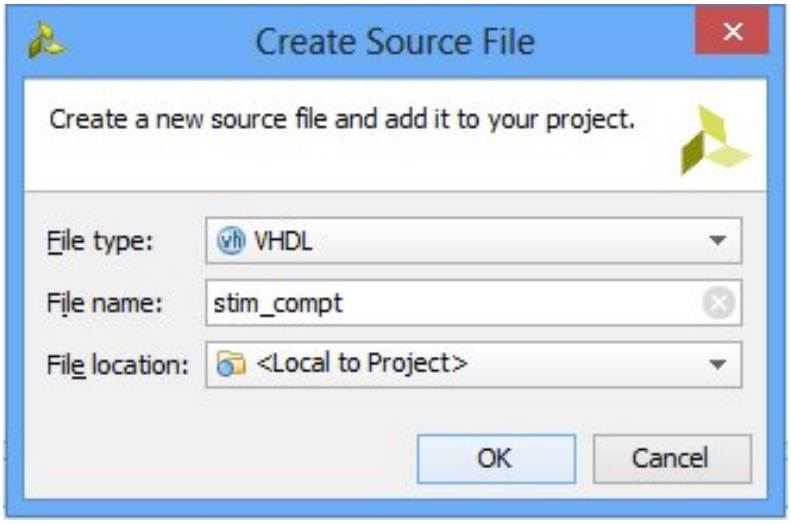


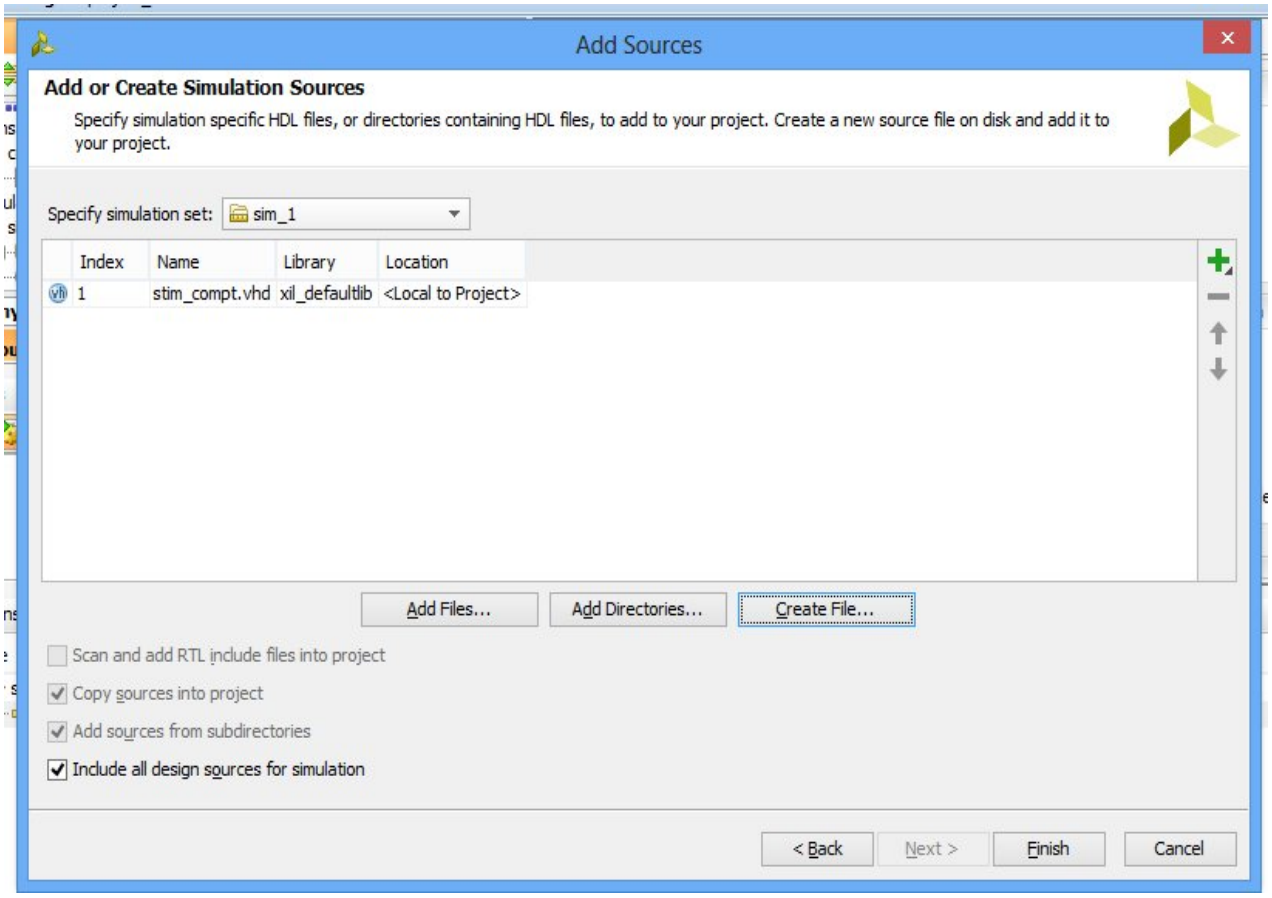


Cliquez sur create file

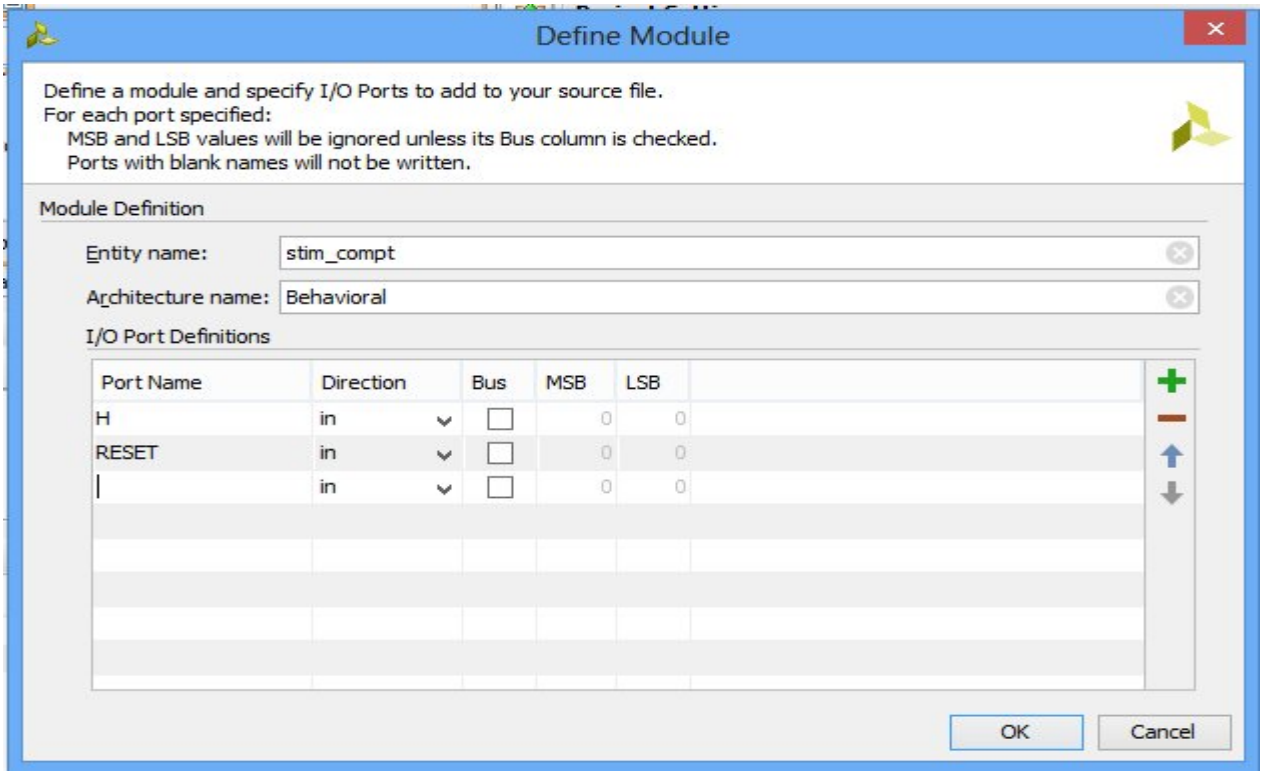


Nommez le fichier stim_compt

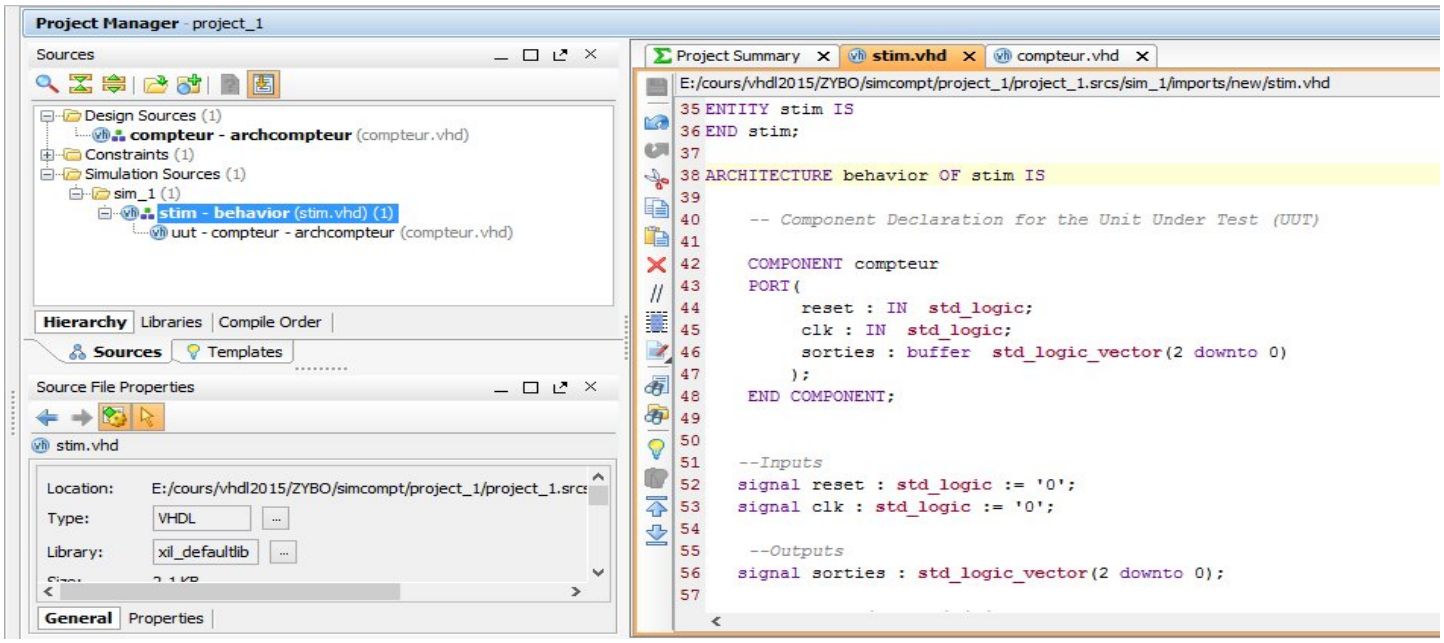




Complétez le nom des signaux pour les stimulis

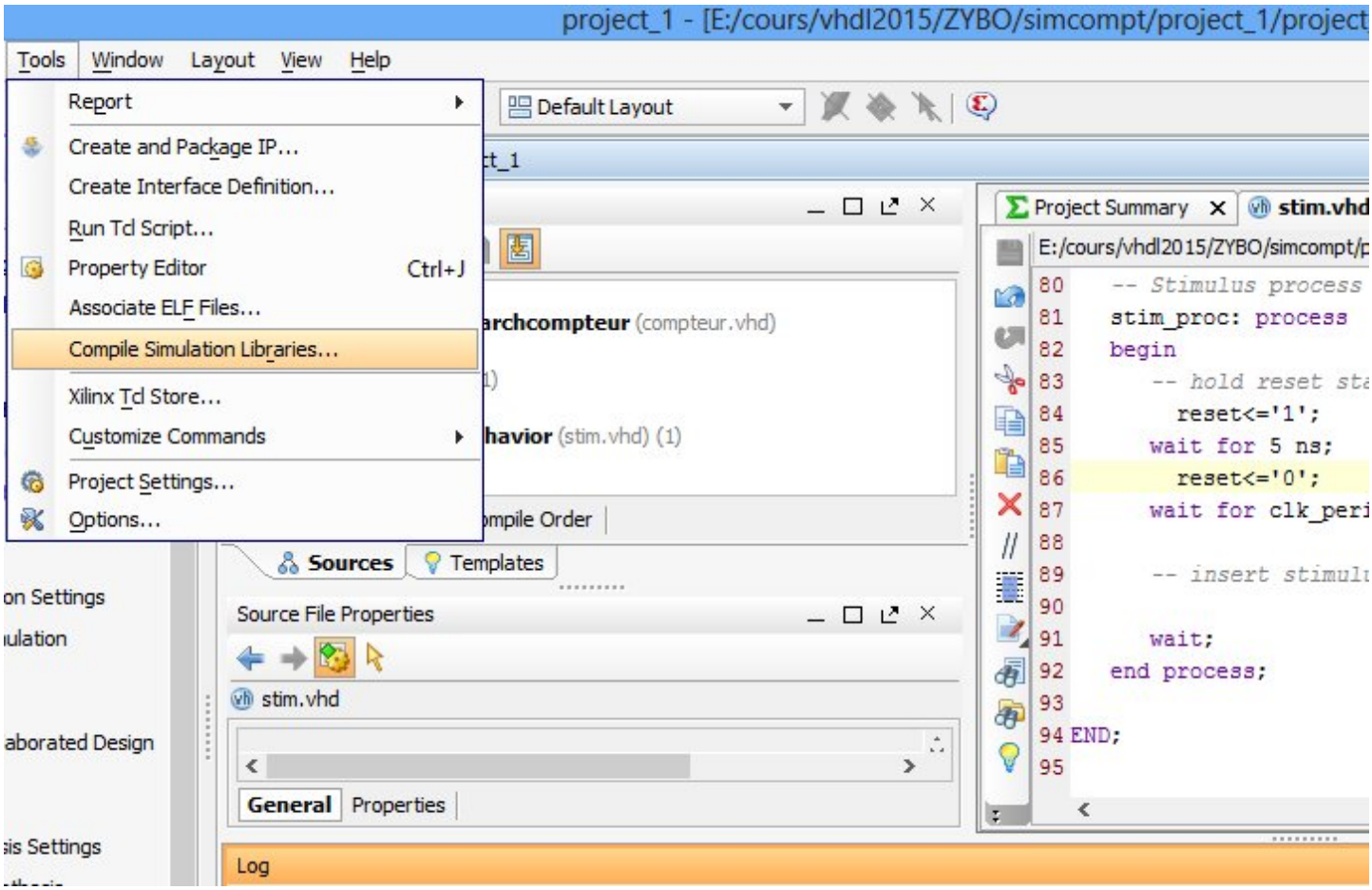


Complétez le fichier de stimuli

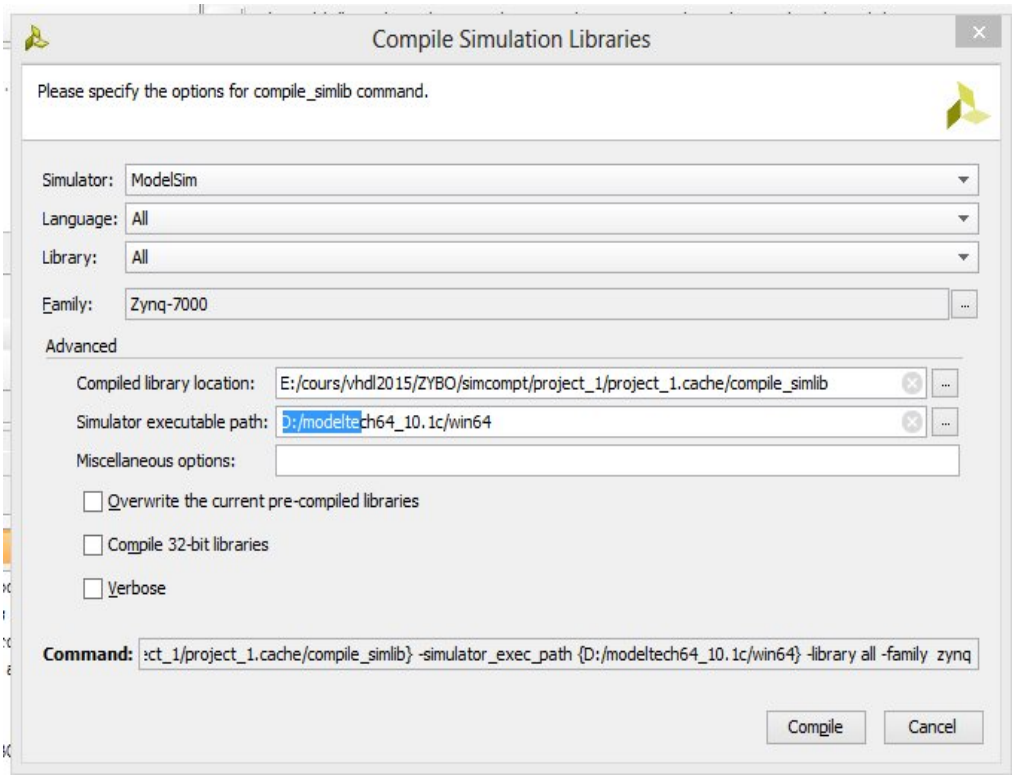


Simulation sous MODELSIM

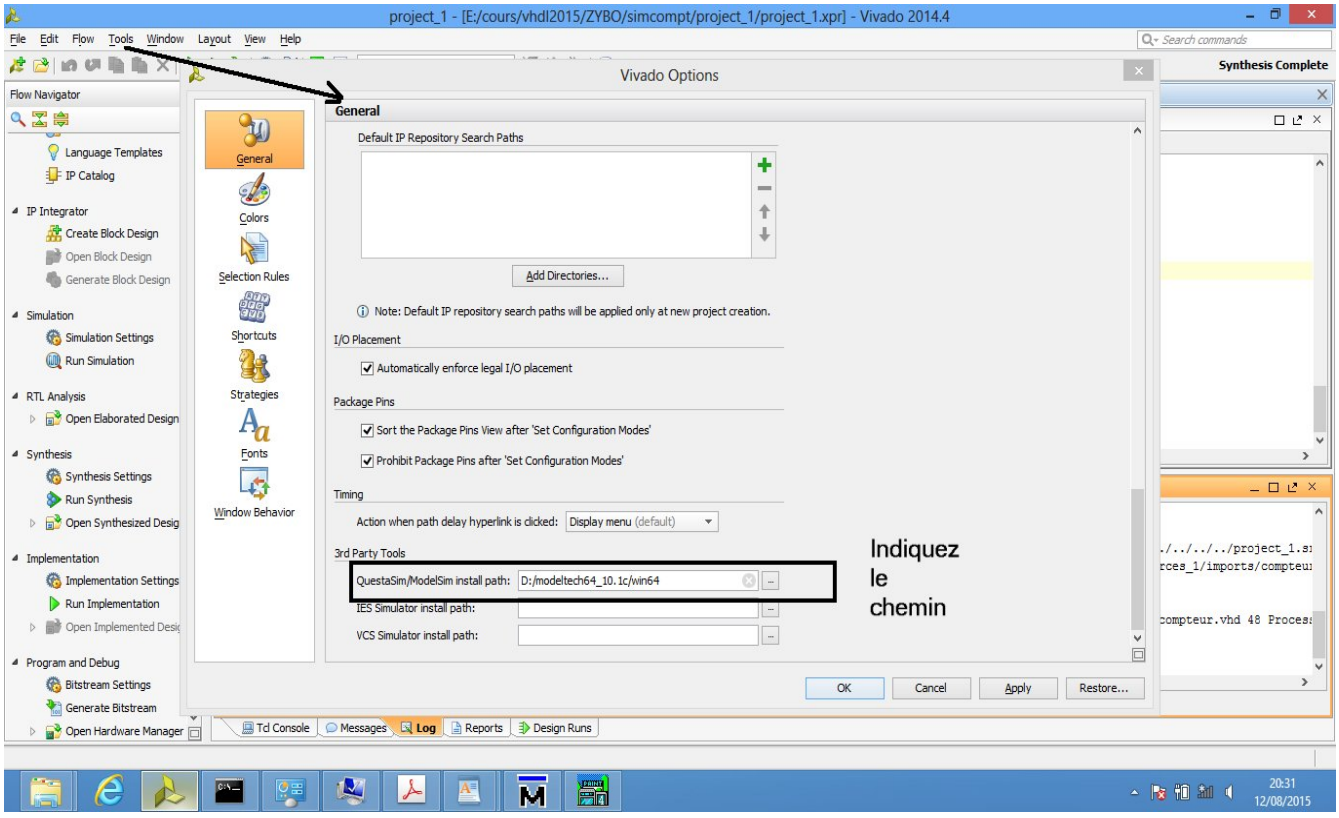
Pour le simulateur MODELSIM, quelques paramétrages sont nécessaires



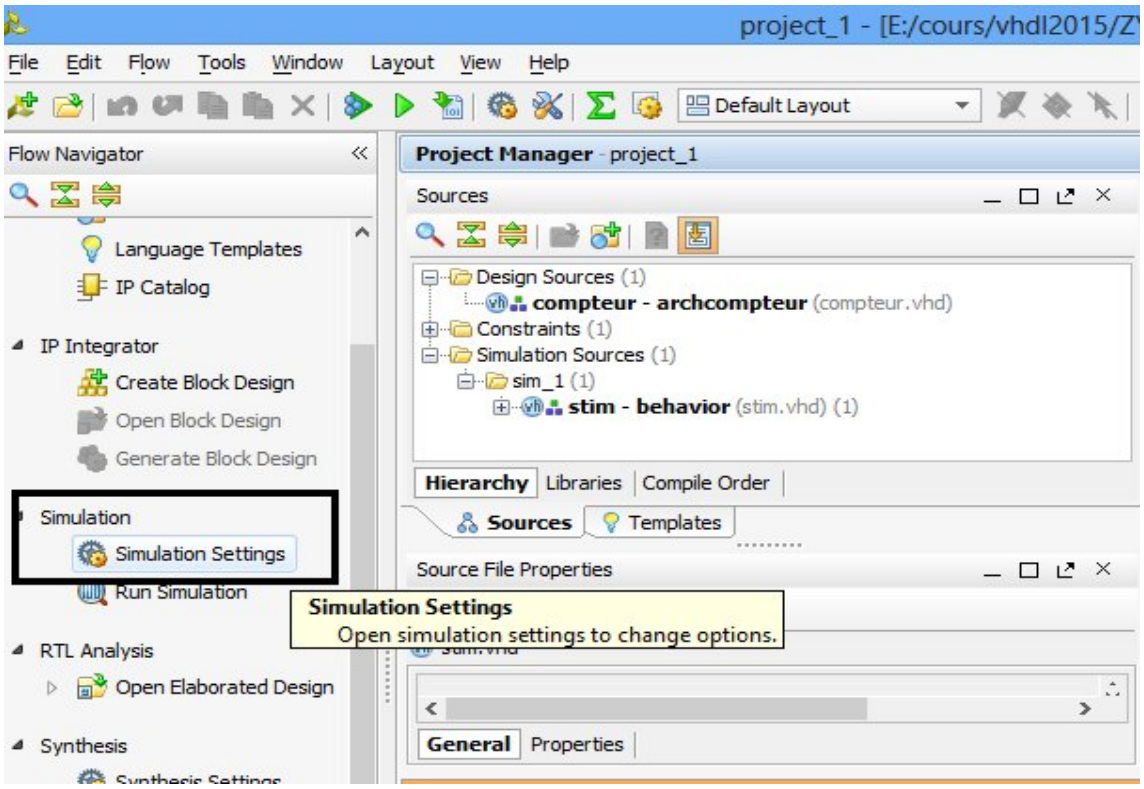
Complétez les champs de la manière suivante

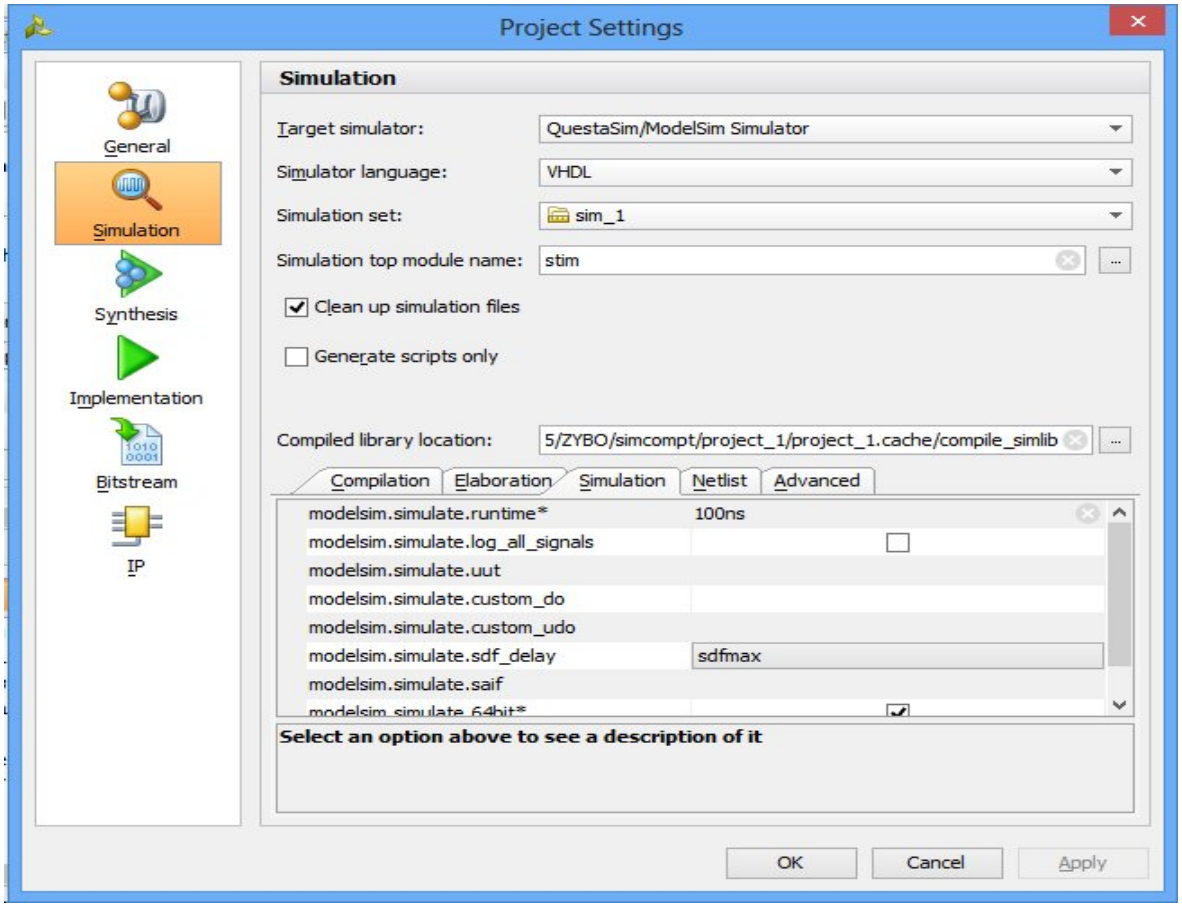


Dans tools→ options et général complétez les champs manquants

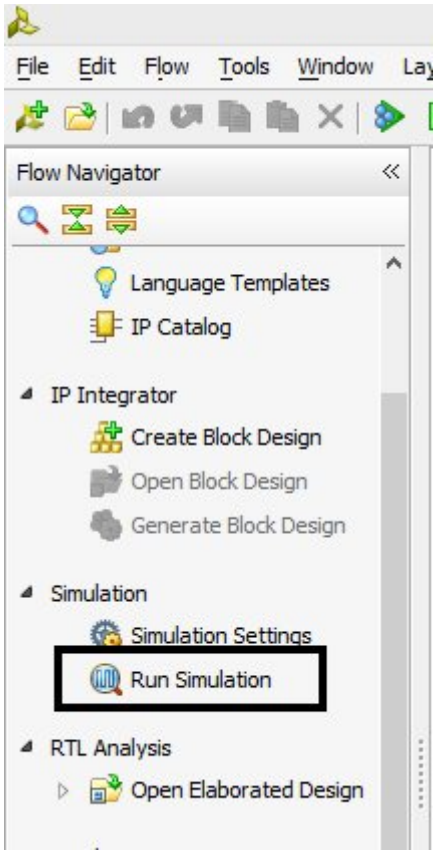


Cliquez sur simulation settings choisir les bon paramètres

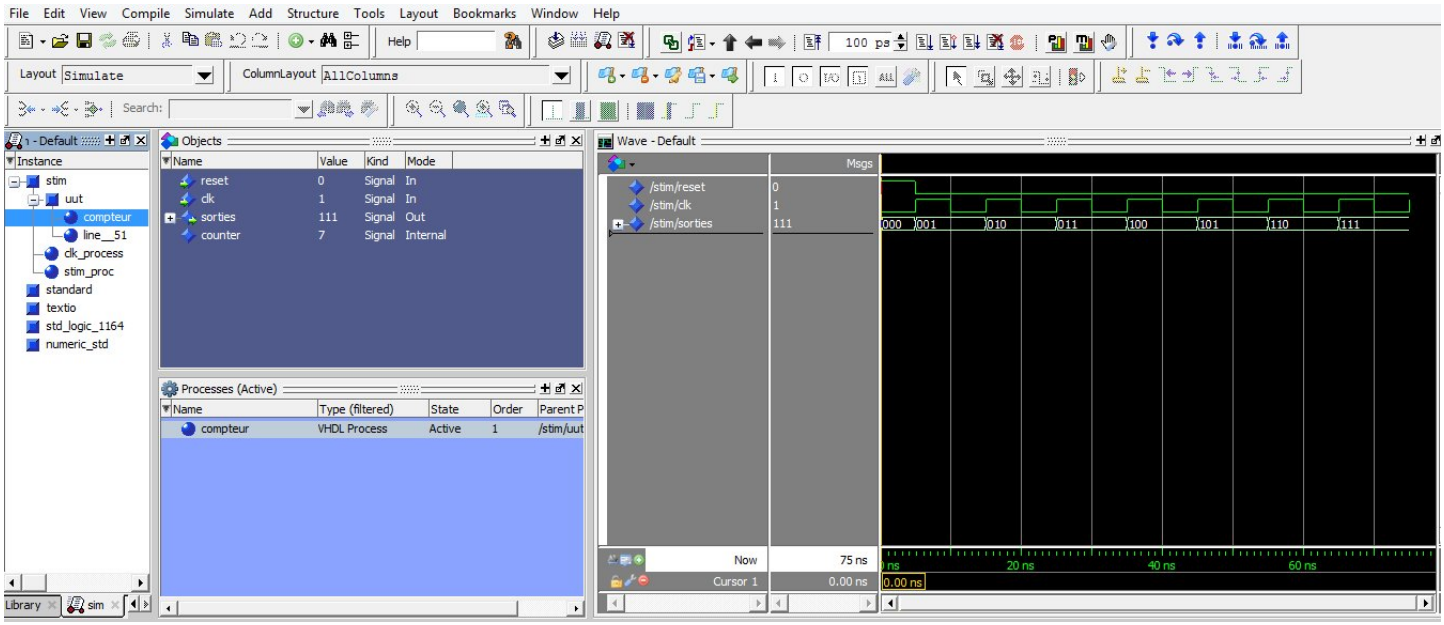




Lancez la simulation

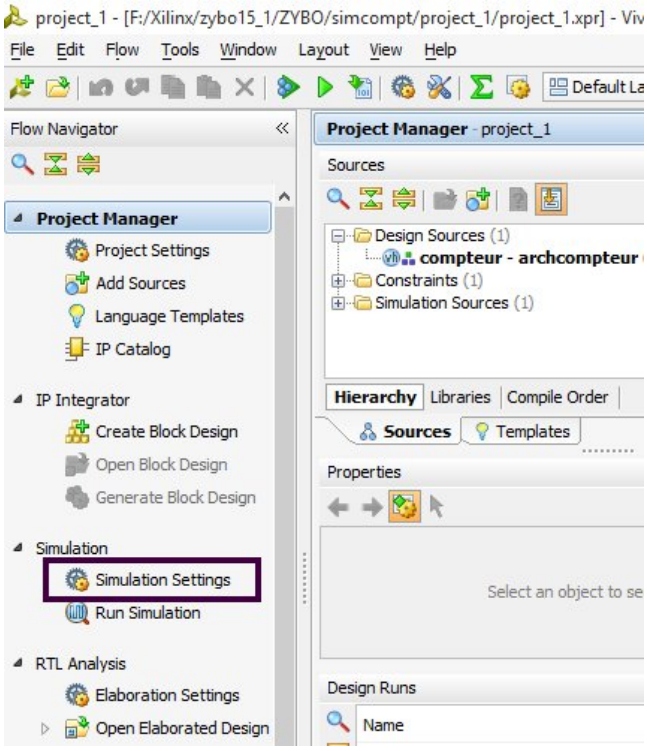


Les résultats apparaissent sous MODELSIM

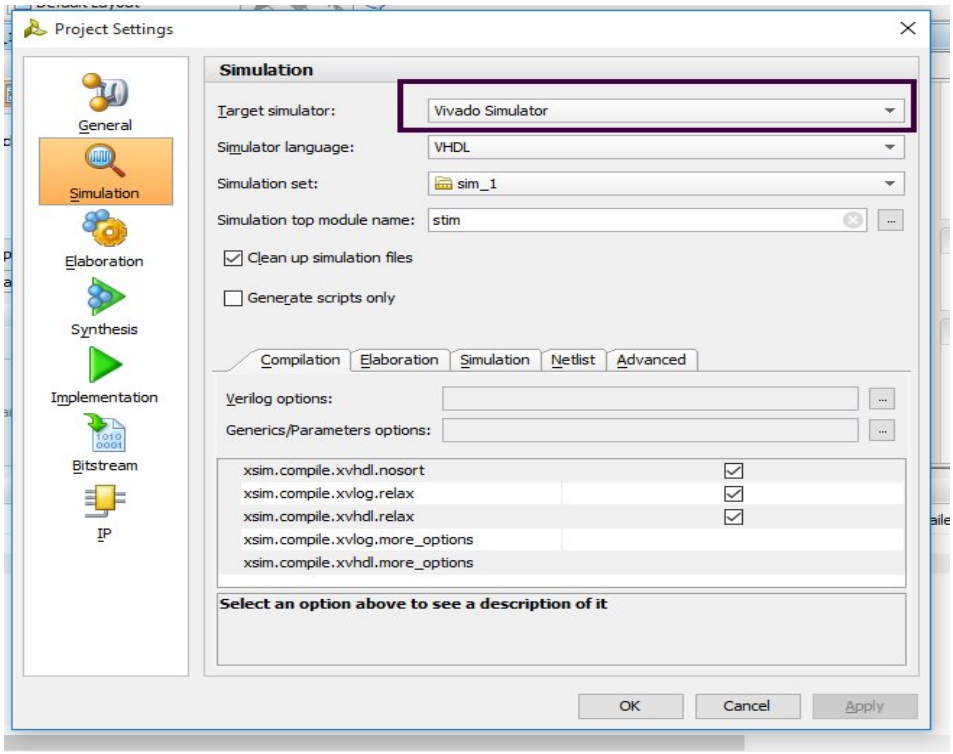


Simulation sous Vivado simulator

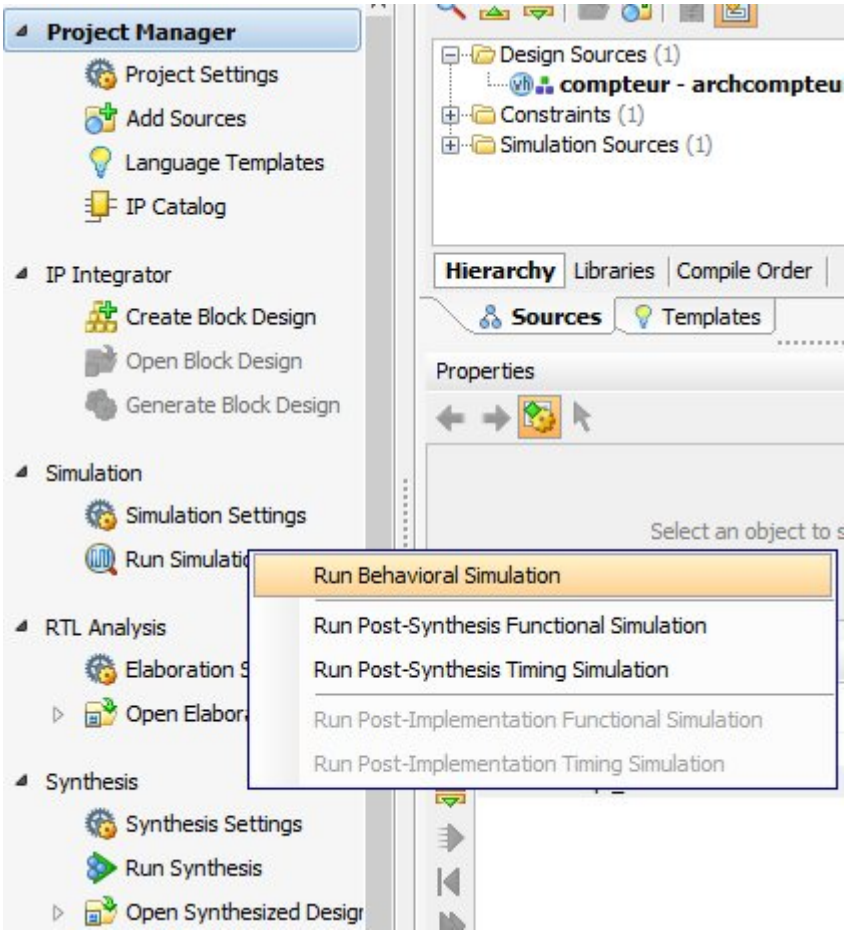
Cliquez sur simulation settings



Sélectionnez le simulateur vivado



Lancez la simulation



Les résultats apparaissent sous Vivado simulator

